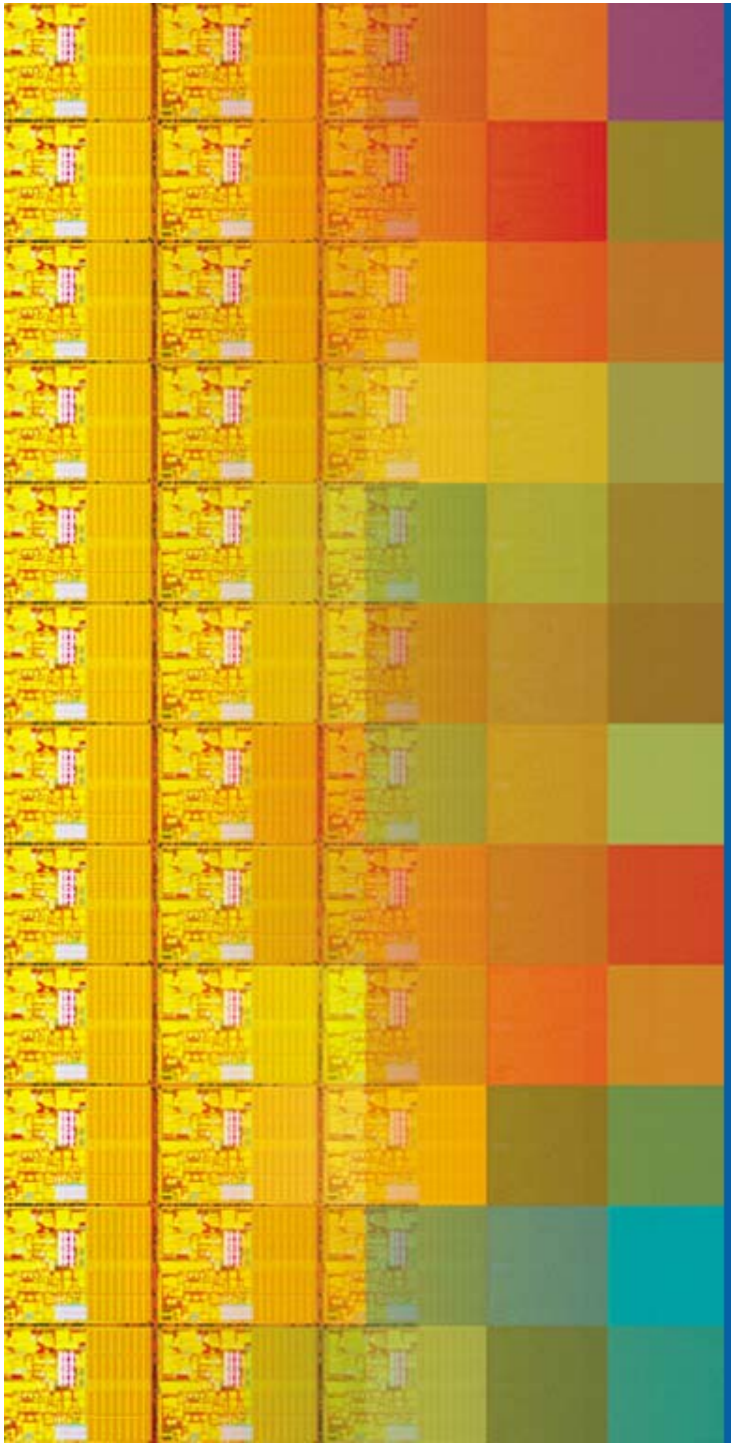

intel Leap ahead™

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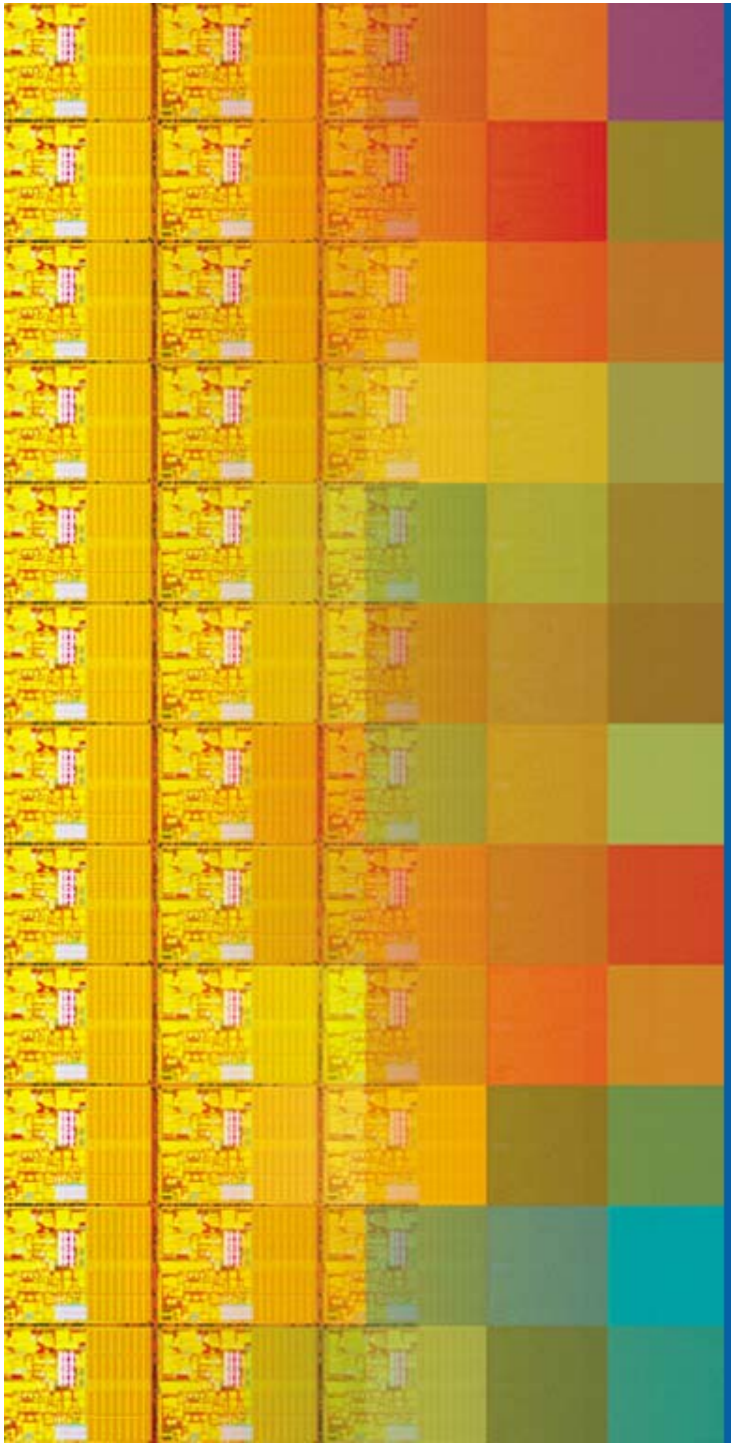


Intel's Silicon R&D Pipeline

Mark Bohr
Intel Senior Fellow
Director of Process Architecture & Integration
Logic Technology Development

Intel Developer FORUM

Key Messages

Only Intel has an effective process technology pipeline

- Follows Moore's Law on 2 year cycle
- 65nm production in Q4'05 (1 year lead)
- 45nm prototype in Q1'06
- Technology options for '07 and beyond

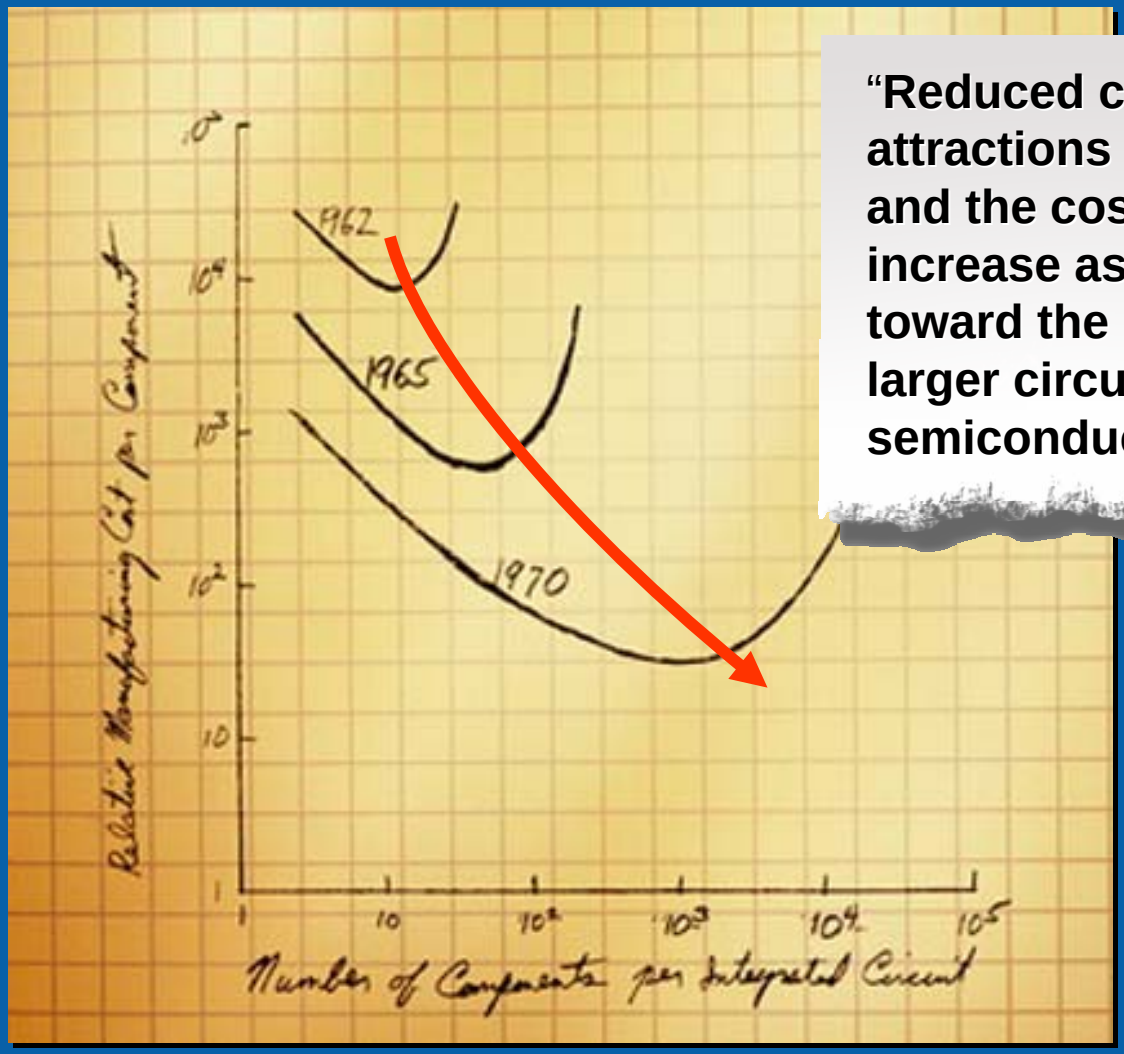
Process technology is an important competitive advantage for Intel platforms

- Industry-leading low leakage transistors provide a solid foundation
- Holistic approach to world class yield, energy efficient performance, and leading-edge capacity

Outline

- Intel's R&D Approach
- What We've Accomplished
- Future Technology Options

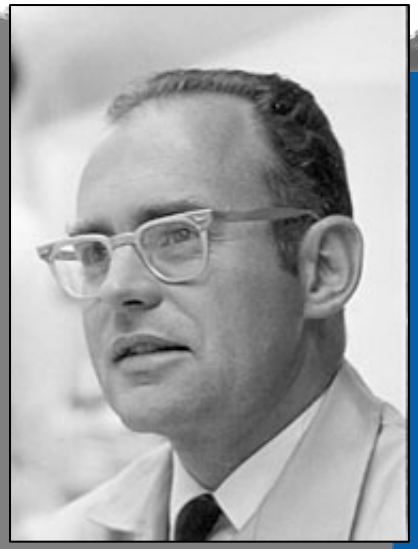
Gordon Moore, 1965



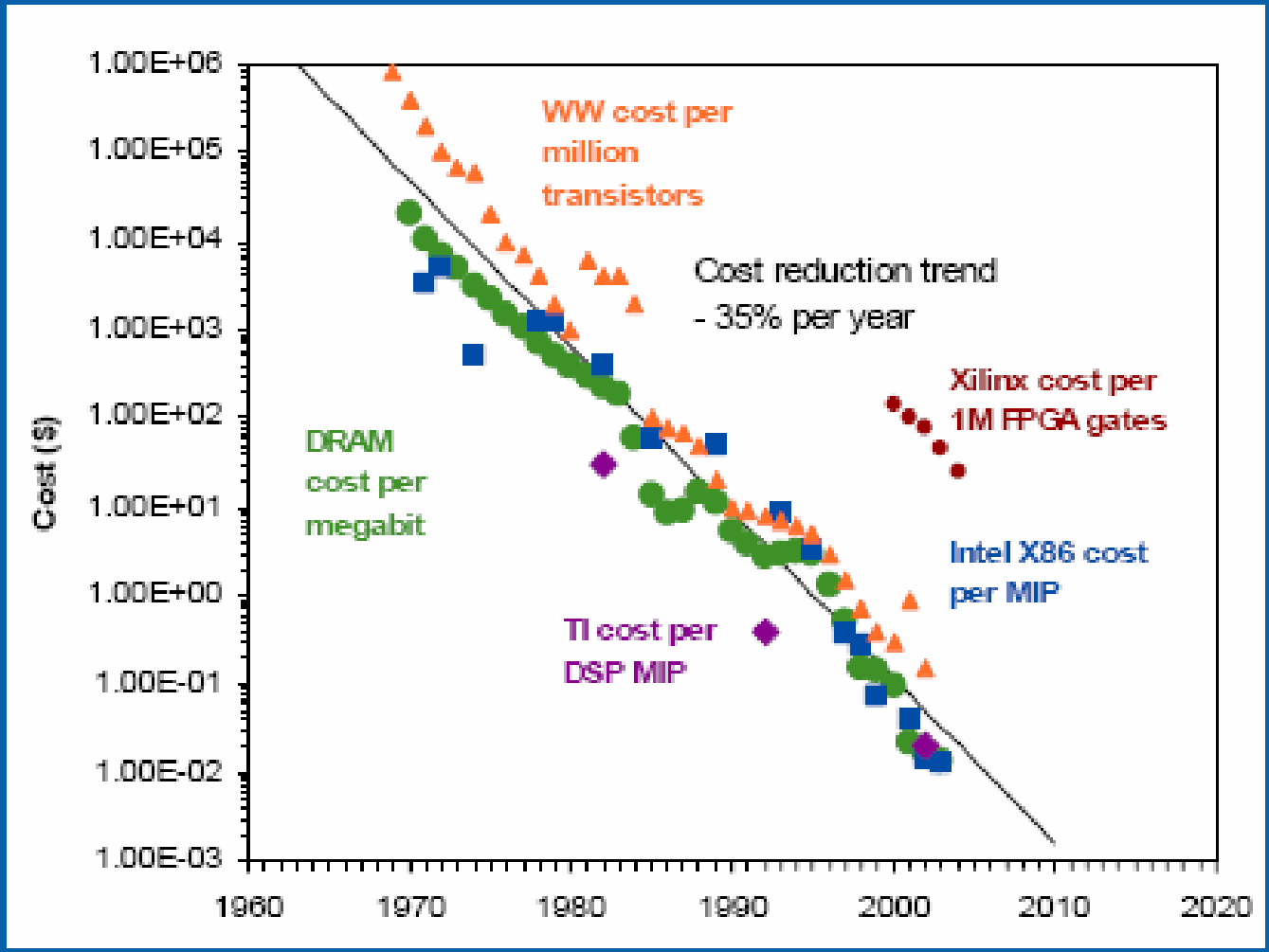
Cost per Component

Number of Components per Chip

"Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate."



Moore's Law Delivers Value to the End User



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Unwavering Commitment to Invest in R&D Pipeline

Research

Identify Ideas/Options

External
- Consortia
- Universities
- Investment
- Suppliers
- Nat'l Labs

Internal
- Oregon

Development

Select Features Make it Work

- Oregon

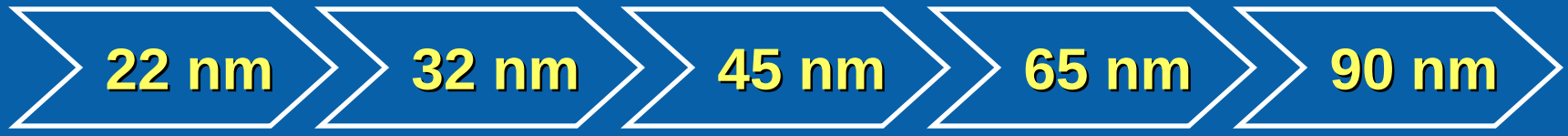
Manufacturing

High Volume Manufacturing

- Oregon
- California
- Arizona
- New Mexico
- Massachusetts
- Israel
- Ireland

Unwavering Commitment to Invest in R&D Pipeline

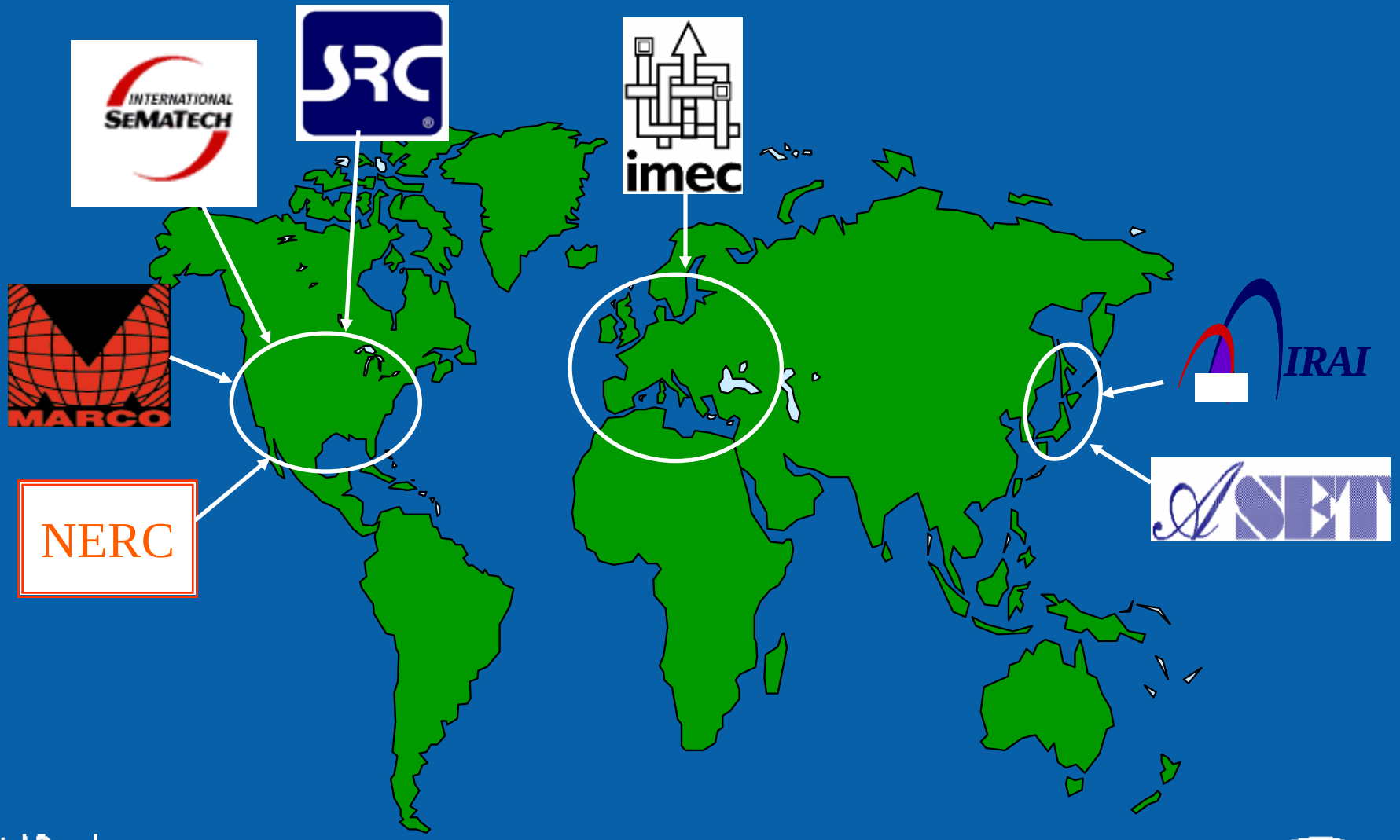
R&D Pipeline



Research Development Manufacturing

Continuous flow of new technologies
from research to manufacturing

Intel Consortia Research Landscape



Intel University Research Landscape

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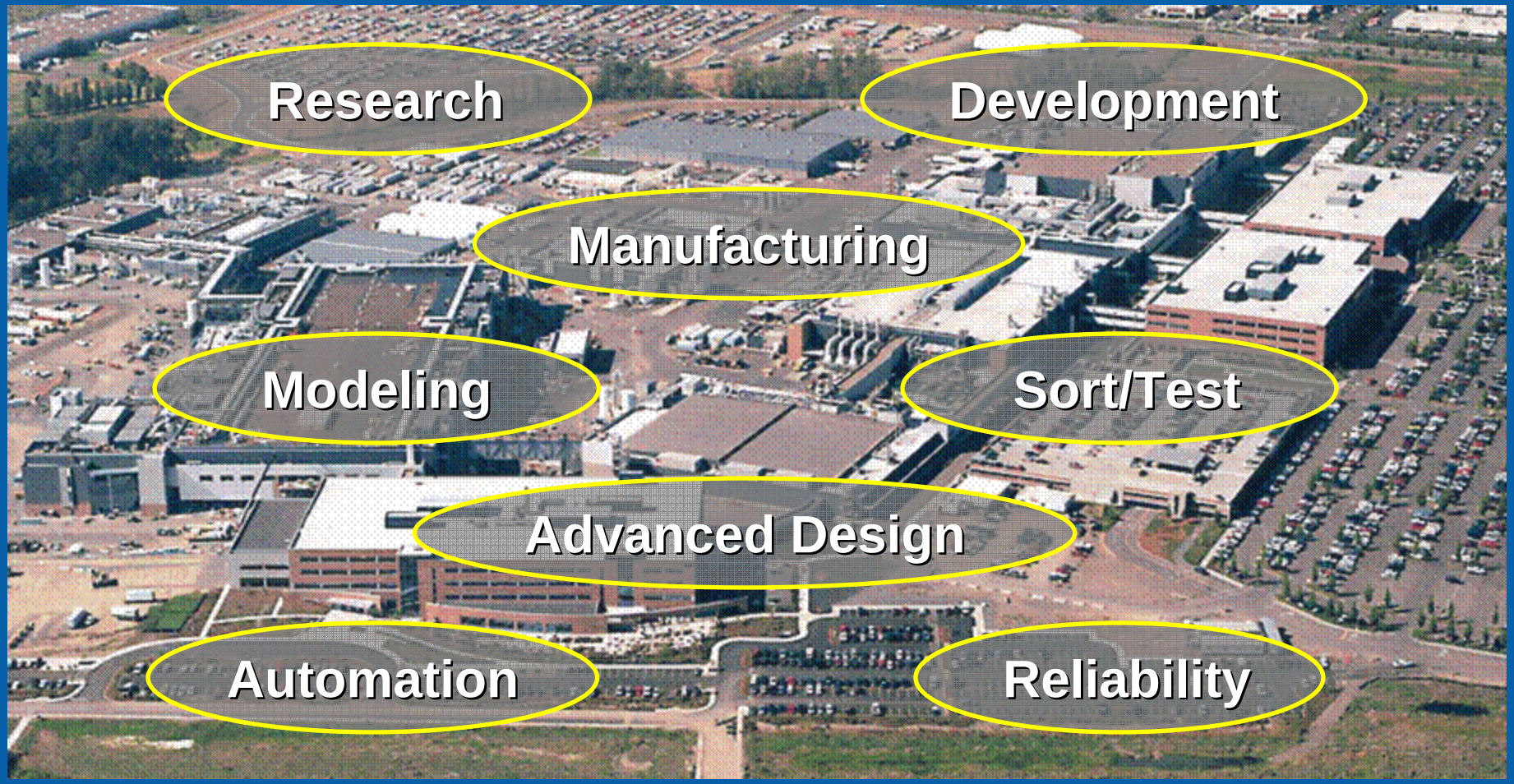
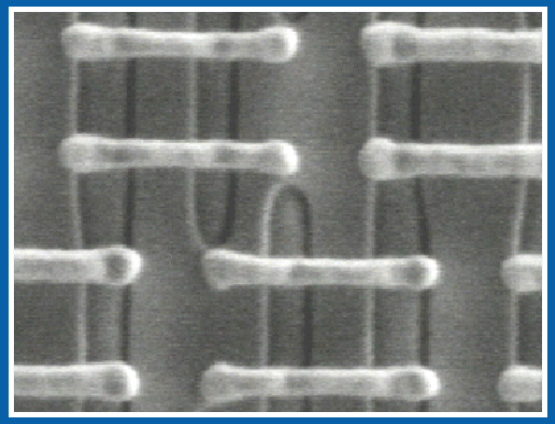
Oregon Campus



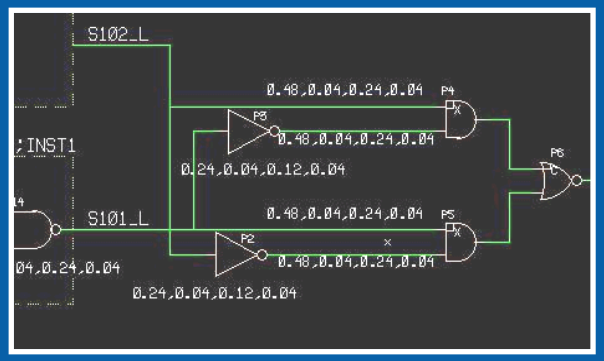
300 mm Research, Development and Manufacturing
All on One Campus

Intel Only:
In-house co-optimization

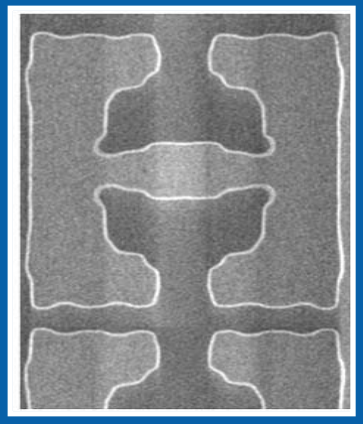


Process

Leading-edge Capacity



Design



Masks

Packaging

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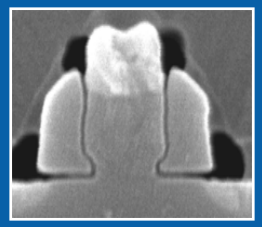
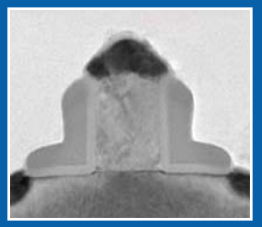
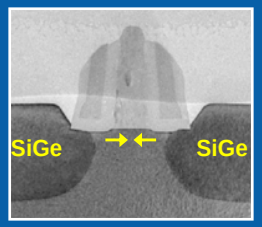
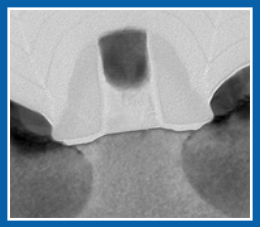
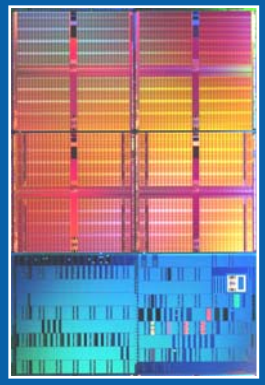
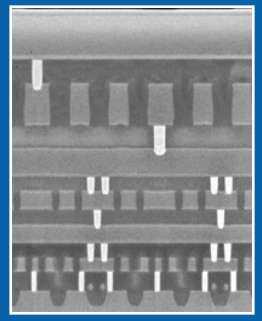
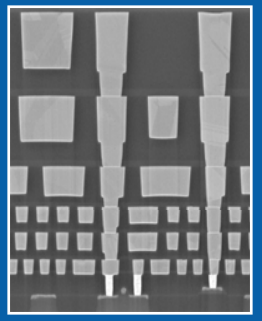
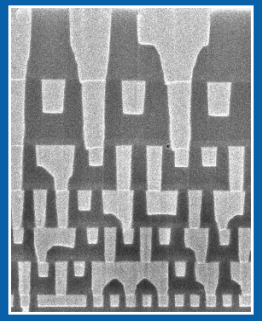
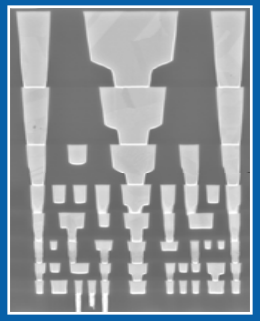
Intel Only:
On-time 2 Year Cycle

	180 nm	130 nm	90 nm	65 nm	45 nm
	1999	2001	2003	2005	2007
Transistor					
Interconnect					
	200mm 100nm L_G $CoSi_2$ 6 Al SiOF	300mm 70nm L_G $CoSi_2$ 6 Cu SiOF	300mm 50nm L_G NiSi Strain Si 7 Cu Low-k	300mm 35nm L_G NiSi 2nd Strain 8 Cu Low-k	Details Coming!

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Outline

- Intel's R&D Approach
- What We've Accomplished
- Future Technology Options

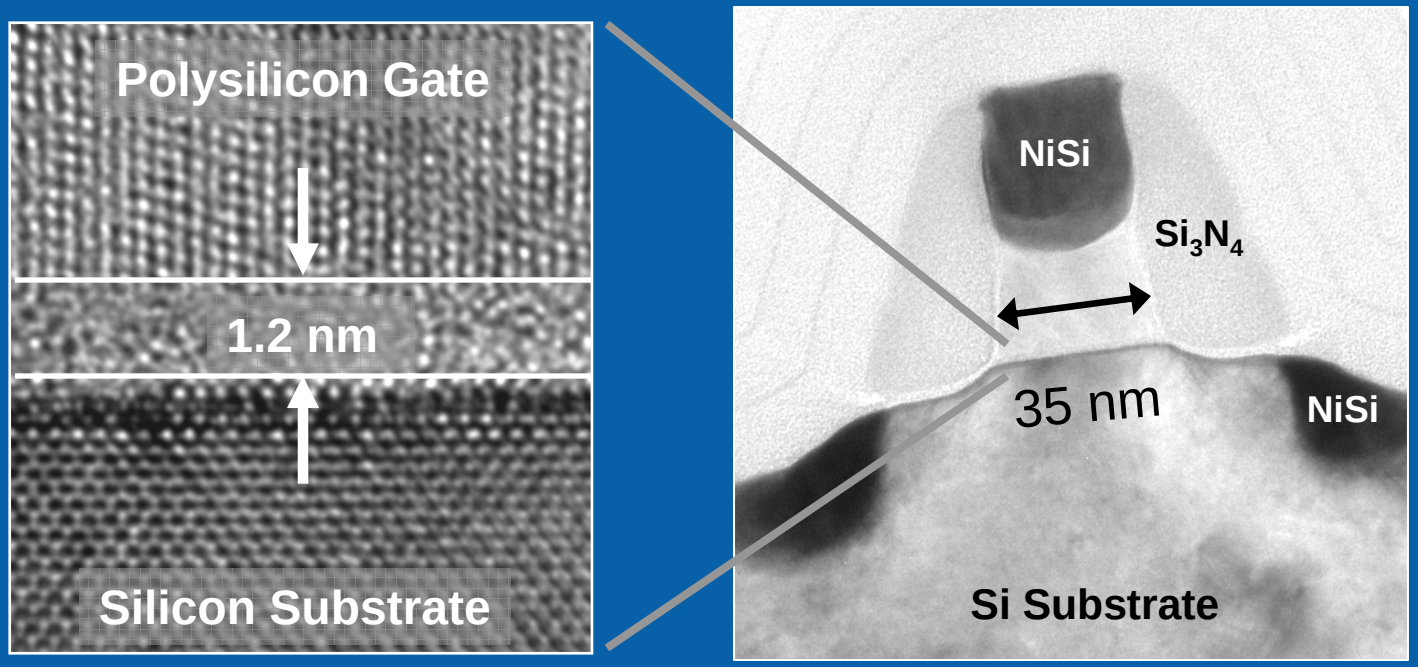
65 nm Logic Technology

Process Name	P1262	P1264	P1266	P1268
Lithography	90 nm	65 nm	45 nm	32 nm
1st Production	2003	2005	2007	2009

Moore's Law continues!

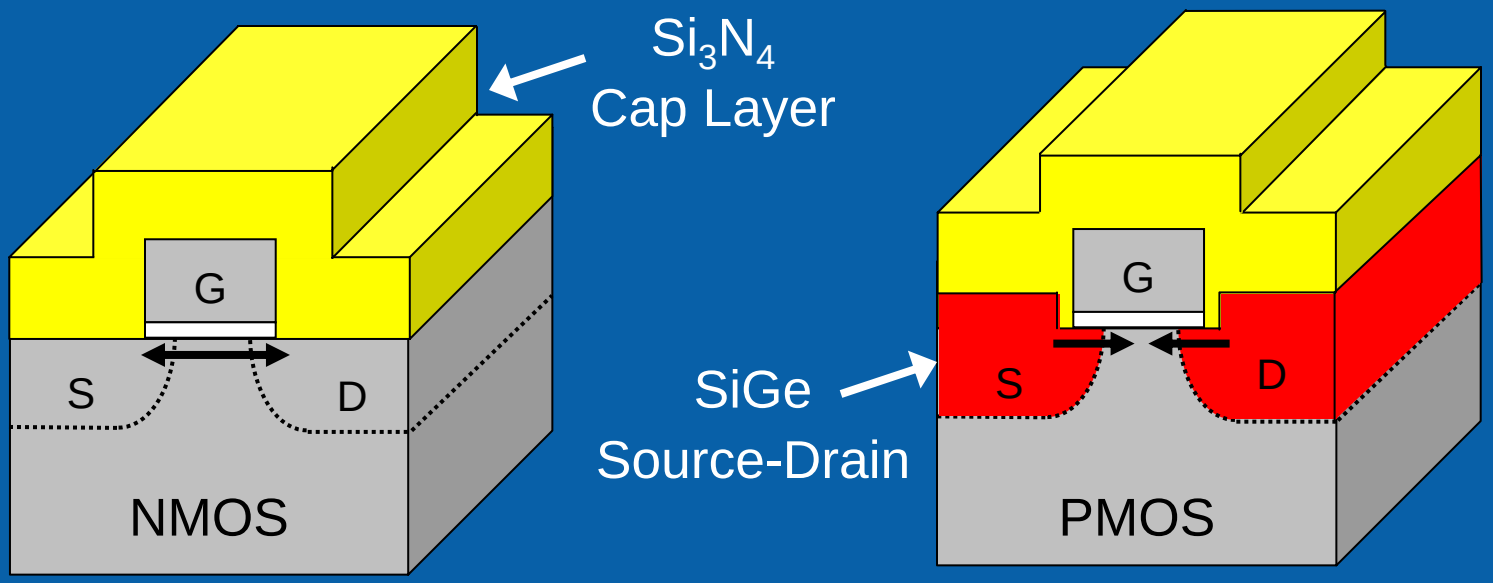
65 nm technology delivered on schedule in 2005

65 nm Transistors



Leading edge transistor technology is unmatched by our competitors

2nd Generation Strained Silicon

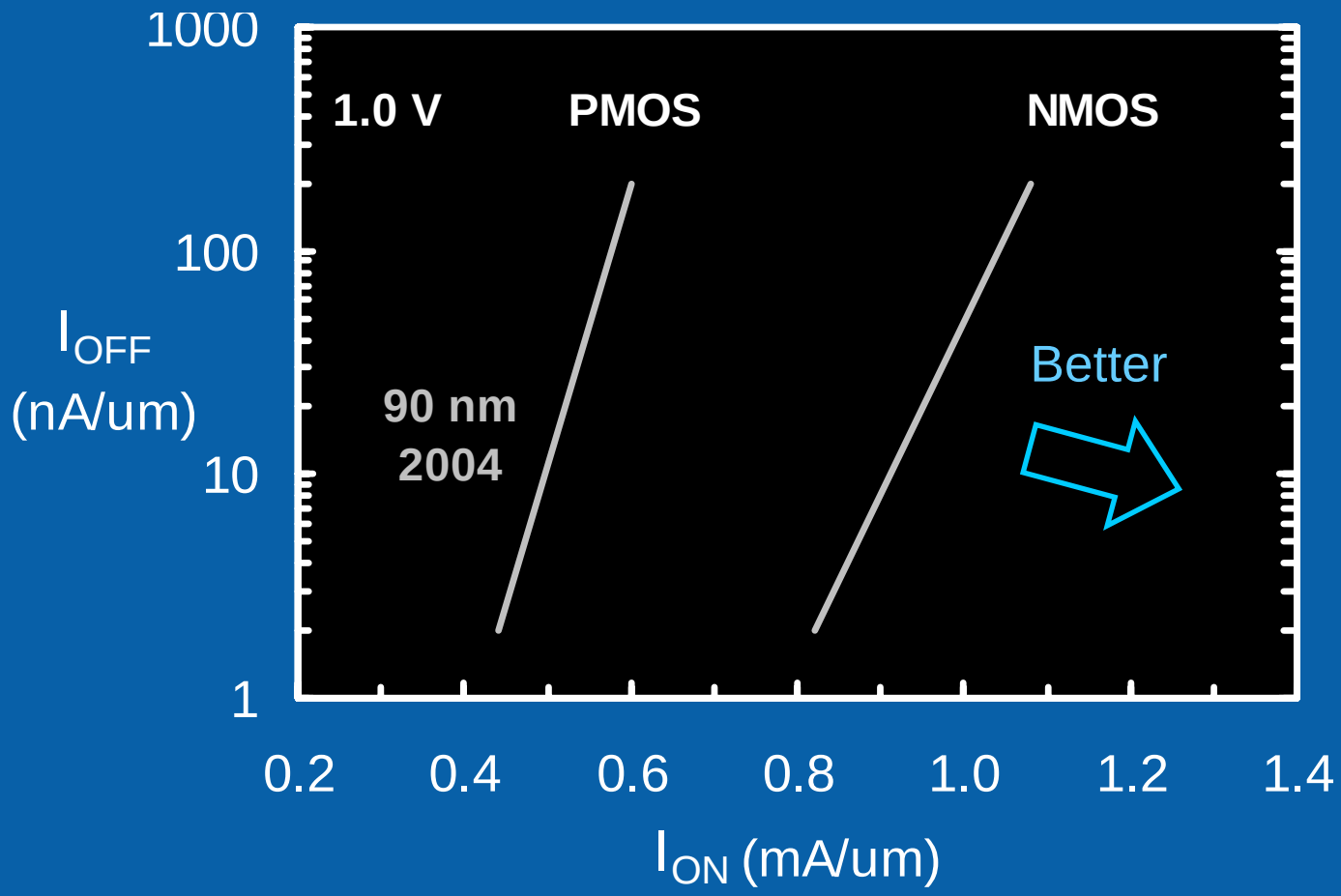


Uniaxial
Tensile Strain

Uniaxial
Compressive Strain

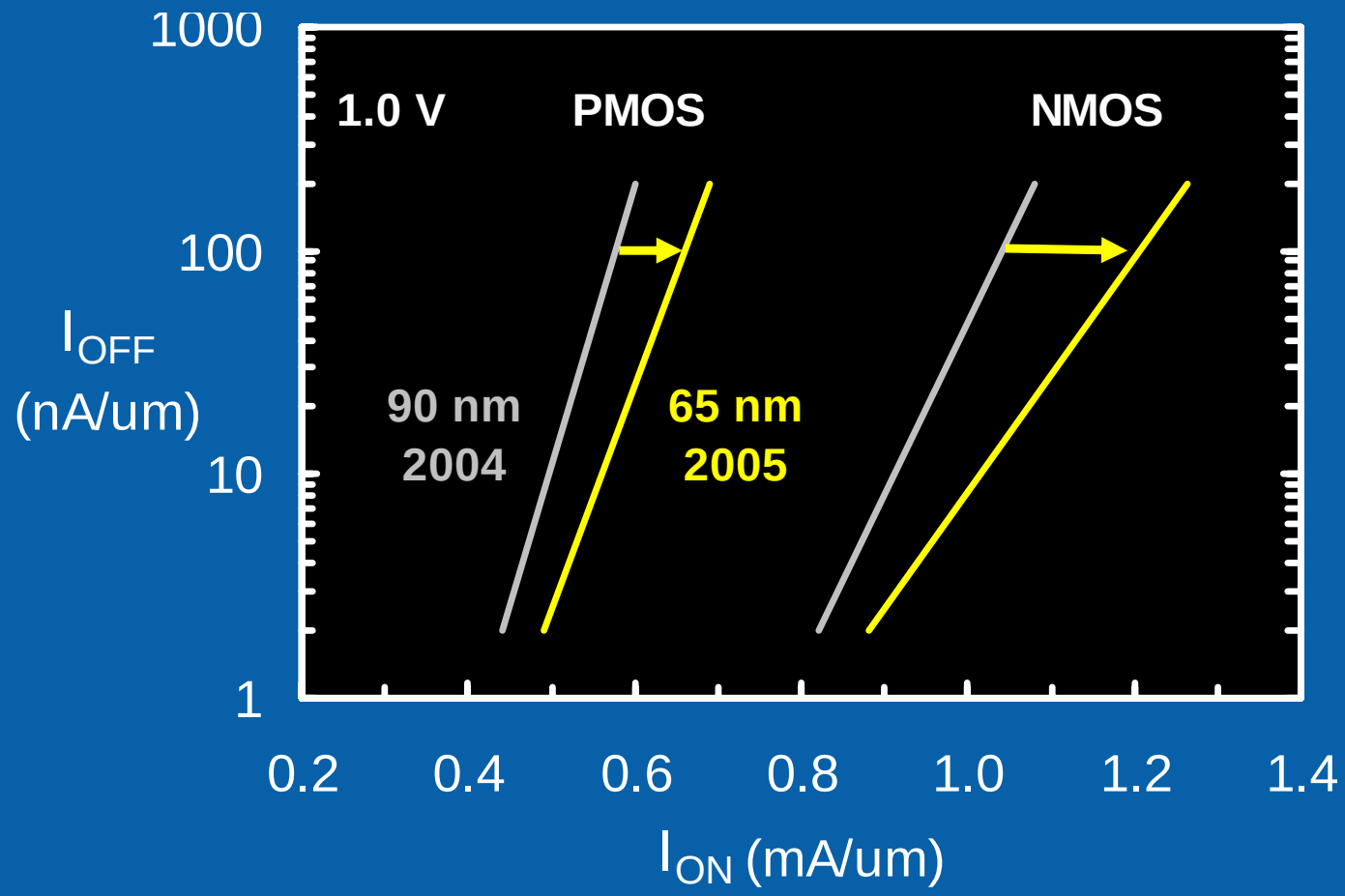
Intel's unique strained silicon technology increases transistor drive current by an average of >30%

Transistor Performance



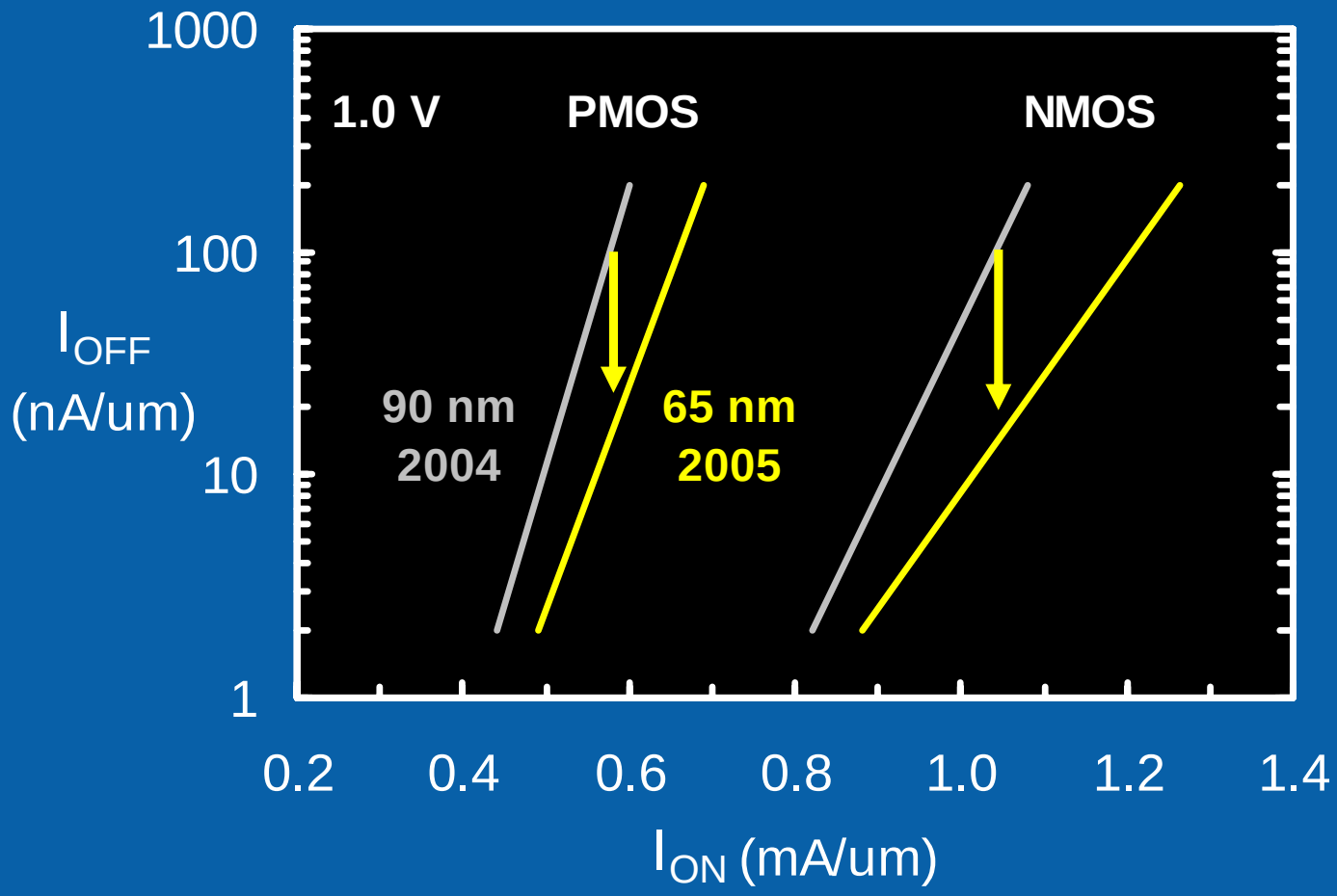
Transistor goal is to increase drive current (I_{ON}) without increasing leakage (I_{OFF})

Transistor Performance



~16% higher drive current + lower gate capacitance improves transistor switching speed by >20%

Transistor Performance



Transistor leakage reduced ~5x at same drive current

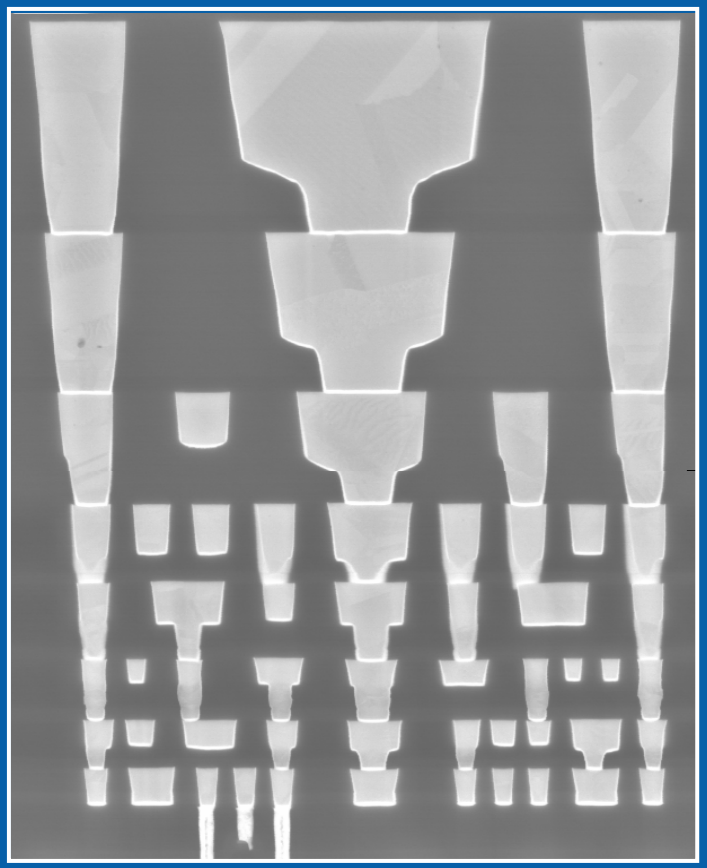
65 nm Interconnects

8 copper interconnect layers

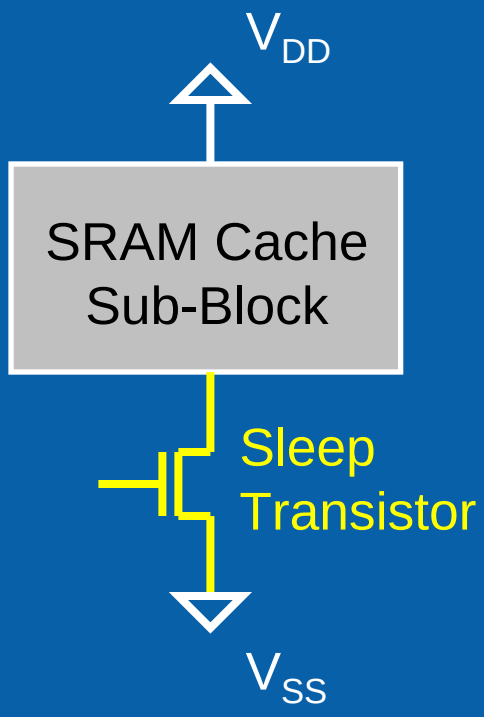
- Dimensions scaled ~0.7x from 90 nm
- Metal 8 layer added for improved density and performance

Low-k carbon doped oxide

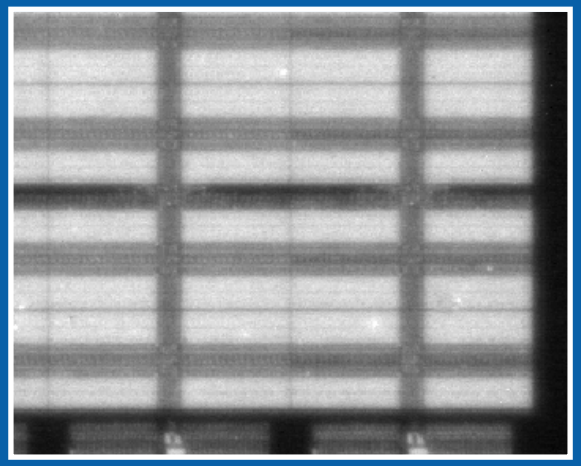
- CDO dielectric reduces interconnect capacitance, improved from 90 nm
- Lower capacitance improves interconnect performance and reduces chip power



Sleep Transistors Reduce SRAM Leakage Power

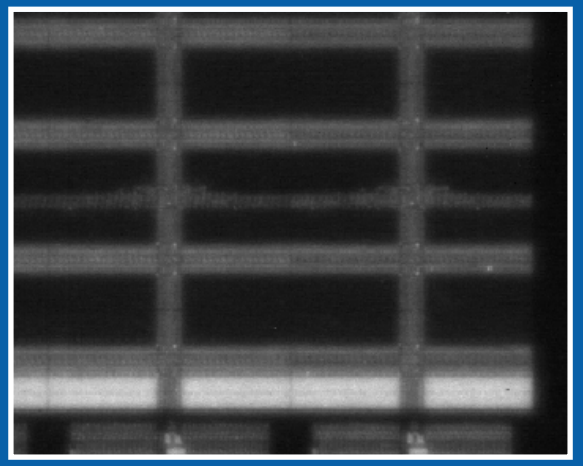


70 Mbit SRAM IR photos



Sleep Transistors On

Normal SRAM leakage



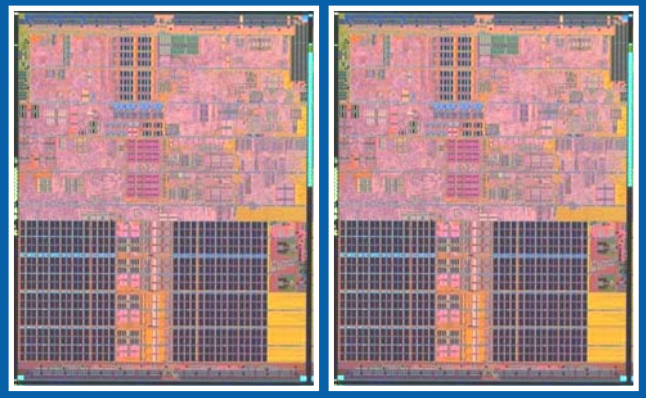
Sleep Transistors Off

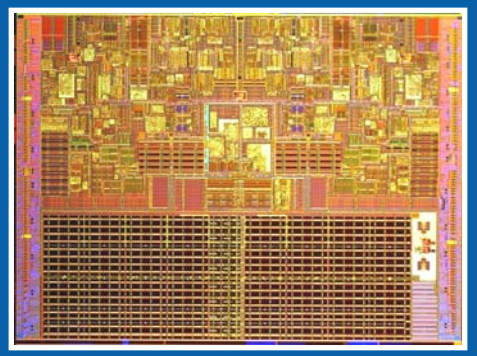
Leakage reduced in inactive sub-blocks

>3x SRAM leakage reduction with use of sleep transistors

65 nm Dual Core CPUs

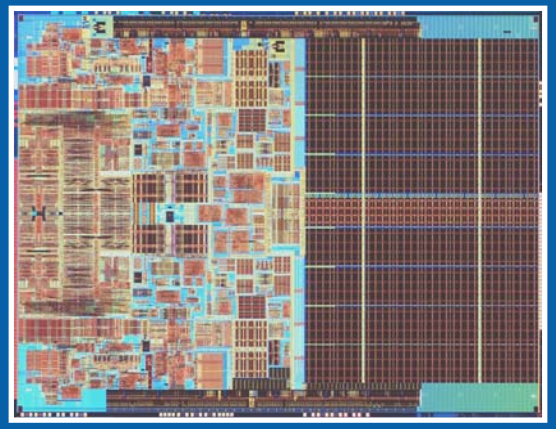
Presler

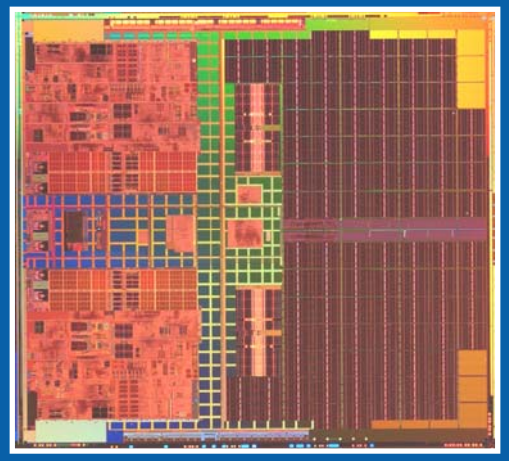




Yonah

Merom





Tulsa

Intel has many 65 nm dual core products

Several million have been shipped to date

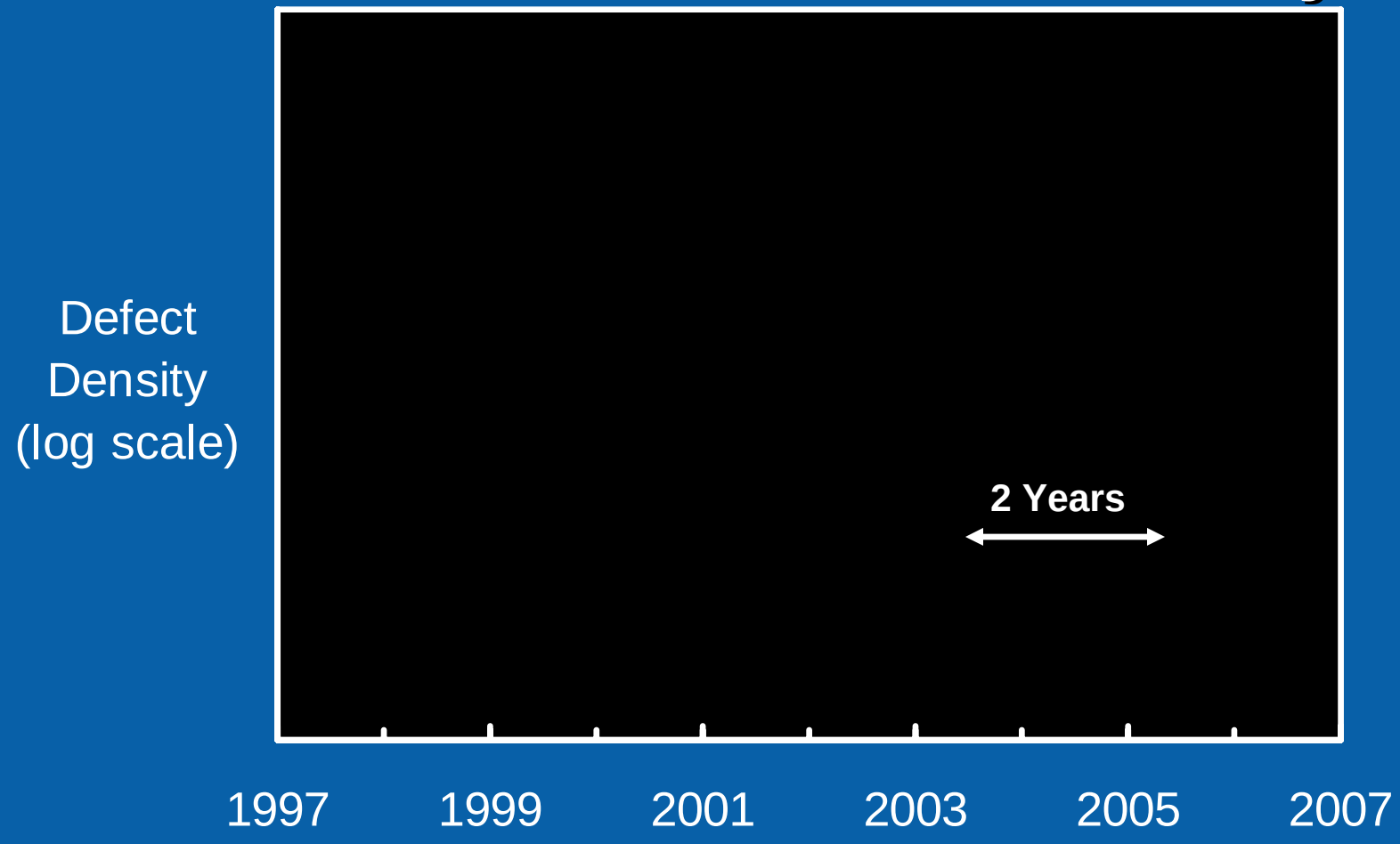
65 nm Manufacturing

65 nm High Volume Fabs

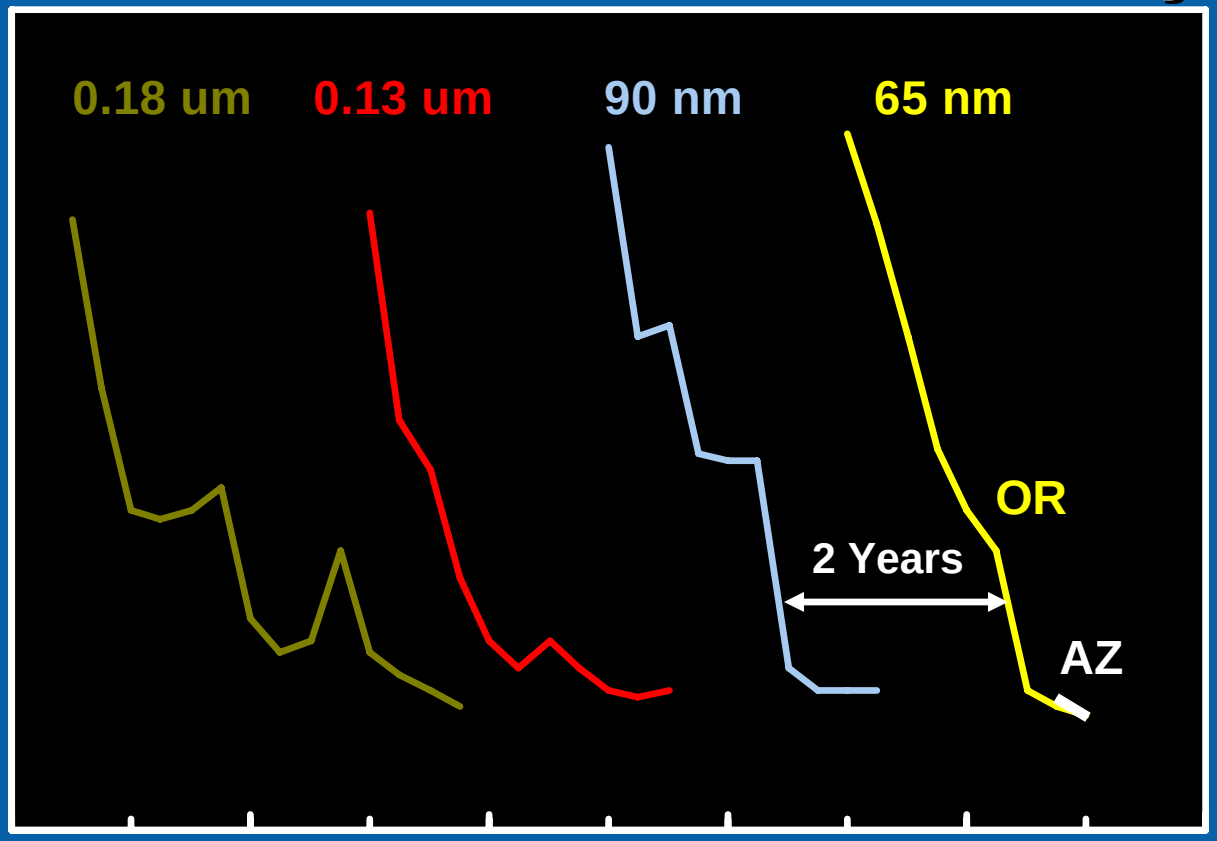
- D1D in Oregon
- F12 in Arizona
- F24 in Ireland, Q2 ’06
- D1C in Oregon, 2H ’06

All 300 mm wafers

Intel Only:
World-Class Yield on 2 Year Cycles



Intel Only:
World-Class Yield on 2 Year Cycles



Defect Density (log scale)

1997 1999 2001 2003 2005 2007

Copy Exactly! transfer methodology enables matched yield at new factory startup

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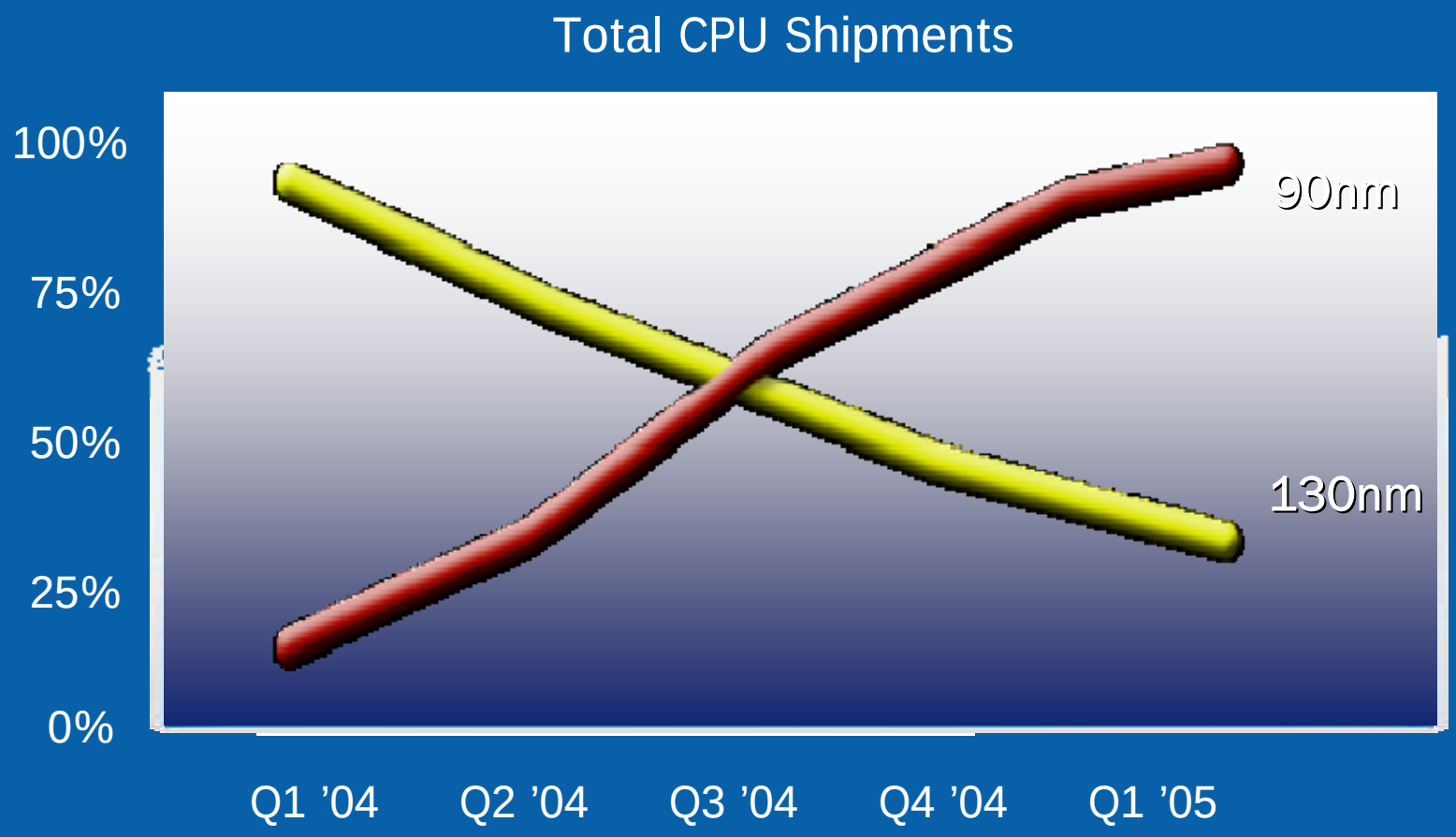
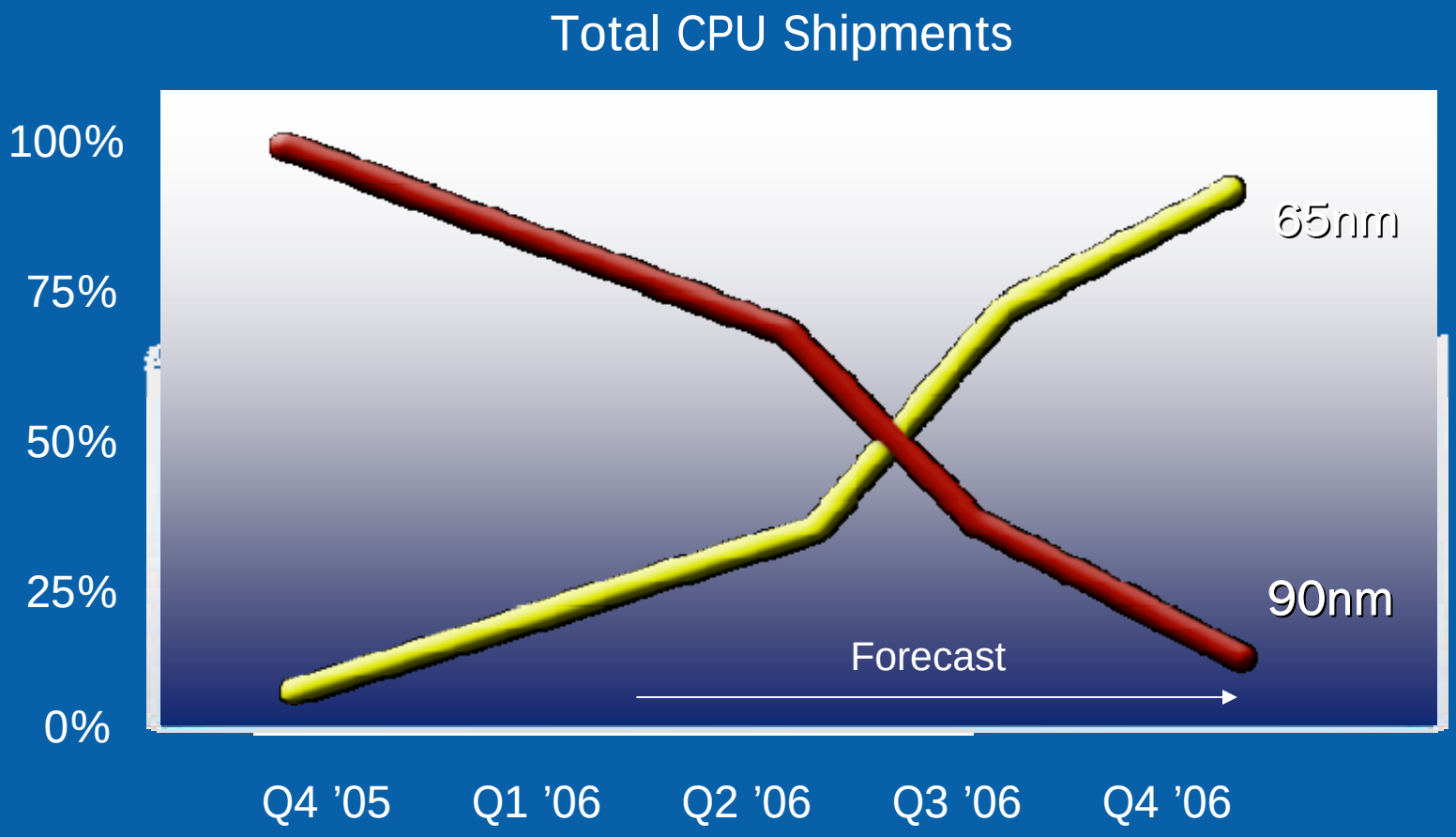
Intel Ahead of Industry on 90 nm Ramp



90 nm crossover occurred in Q3 '04

Intel Only: 65 nm
Process + Products + Production



65 nm crossover projected for Q3 '06

65 nm Summary

- Only Intel has been shipping 65 nm processors since October 2005
- Only Intel has shipped several million 65 nm dual-core processors
- Only Intel has two 65 nm / 300 mm fabs shipping in volume, with two more coming in 2006

Fab Video

45 nm Logic Technology

Process Name	P1262	P1264	P1266	P1268
Lithography	90 nm	65 nm	45 nm	32 nm
1st Production	2003	2005	2007	2009

Moore's Law continues!

45 nm technology on track for delivery in 2007

45 nm Technology Benefits

Compared to today's 65 nm technology, 45 nm will provide the following product benefits:

~2x improvement in transistor density, for either smaller chip size or increased transistor count

>20% improvement in transistor switching speed or **>5x** reduction in leakage power

>30% reduction in transistor switching power

This process technology will provide the foundation to deliver improved performance per watt

45 nm SRAM Chip

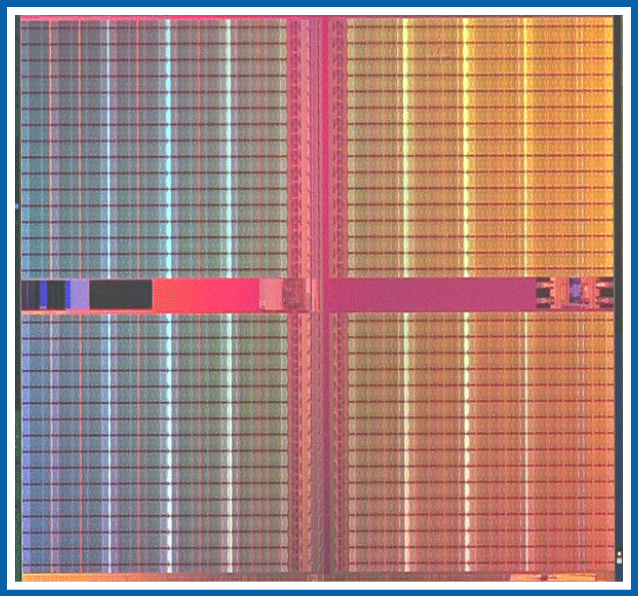
Fully functional silicon in Jan '06

0.346 μm^2 cell

153 Mbit density

119 mm^2 chip size

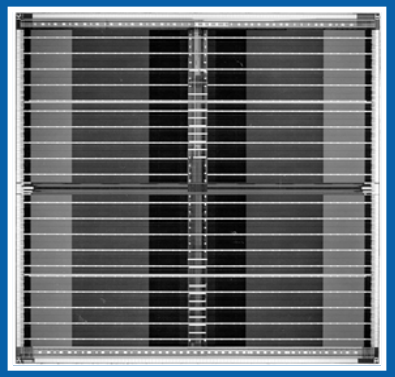
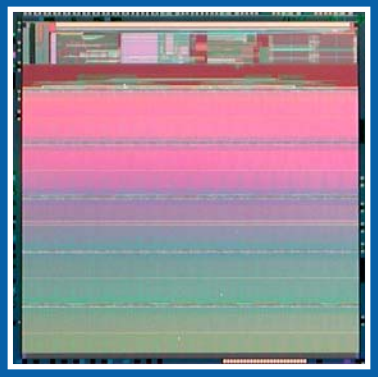
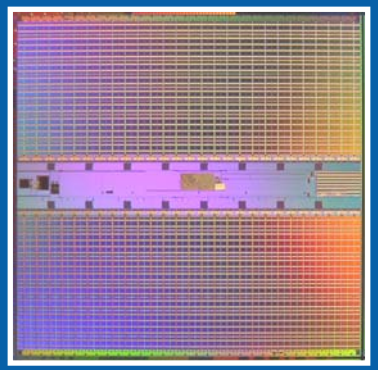
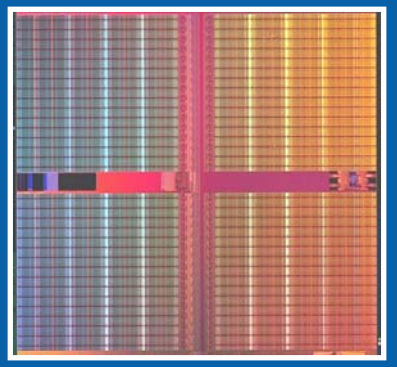
>1 billion transistors



45 nm SRAM test vehicle includes all transistor and interconnect features to be used on 45 nm microprocessors

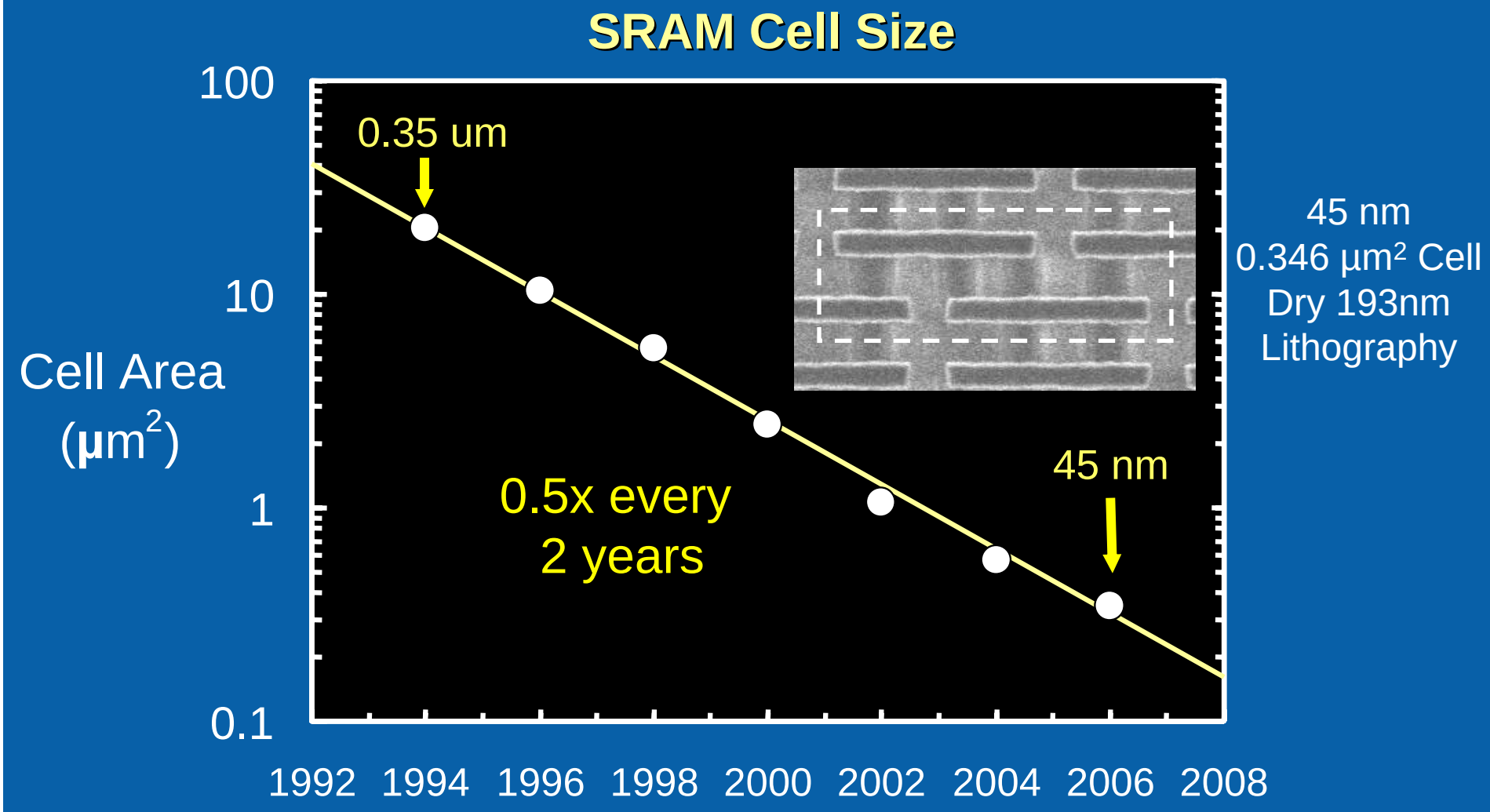
No other company is capable of making a 45 nm SRAM with the density and features we have until 2007 or later

Intel SRAM Test Chips

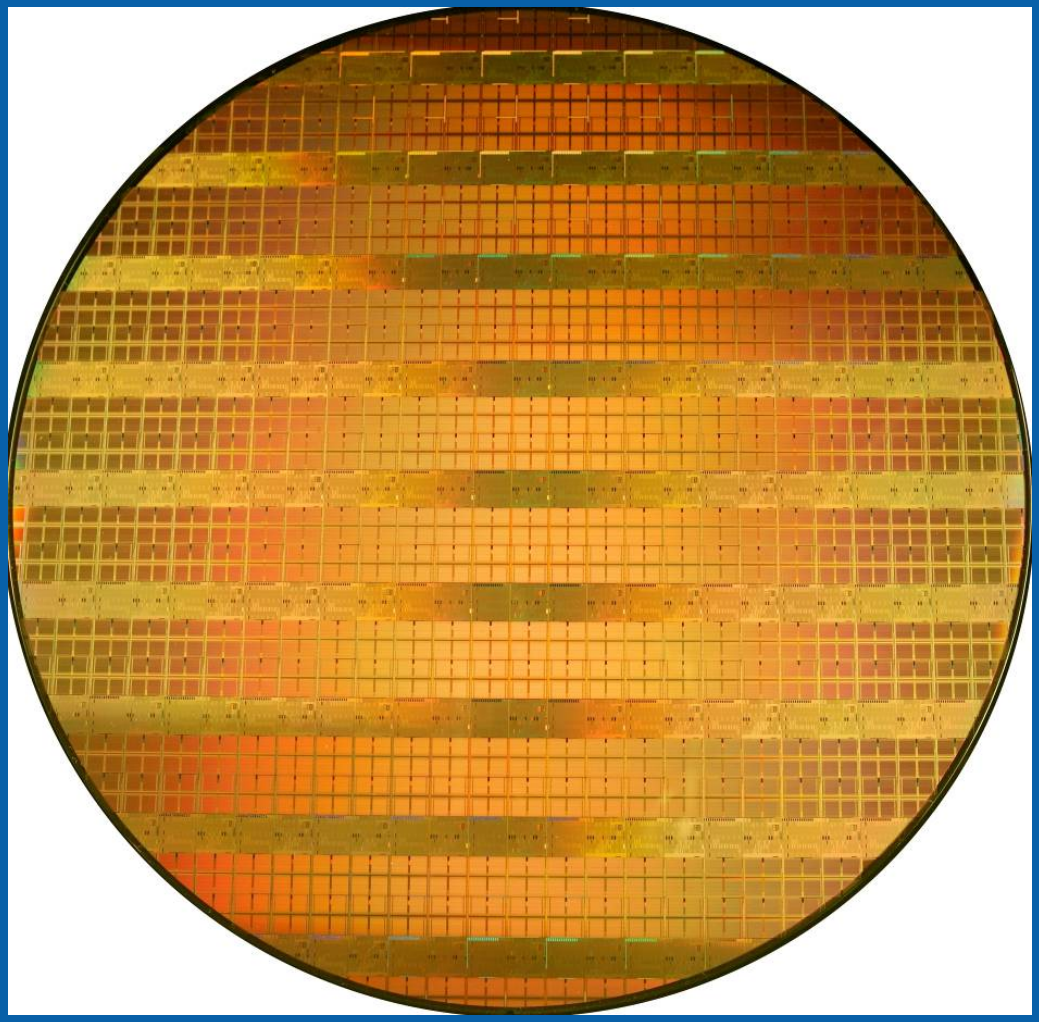
130 nm	90 nm	65 nm	45 nm
			
2.45 μm² cell	**1.0 μm² cell**	**0.57 μm² cell**	**0.346 μm² cell**
18 Mbit	**50 Mbit**	**70 Mbit**	**153 Mbit**
103 mm²	**109 mm²**	**110 mm²**	**119 mm²**
March '00	**February '02**	**April '04**	**January '06**

New SRAM test vehicle developed every
2 years to lead development of logic technologies

Intel's Density Scaling on Track



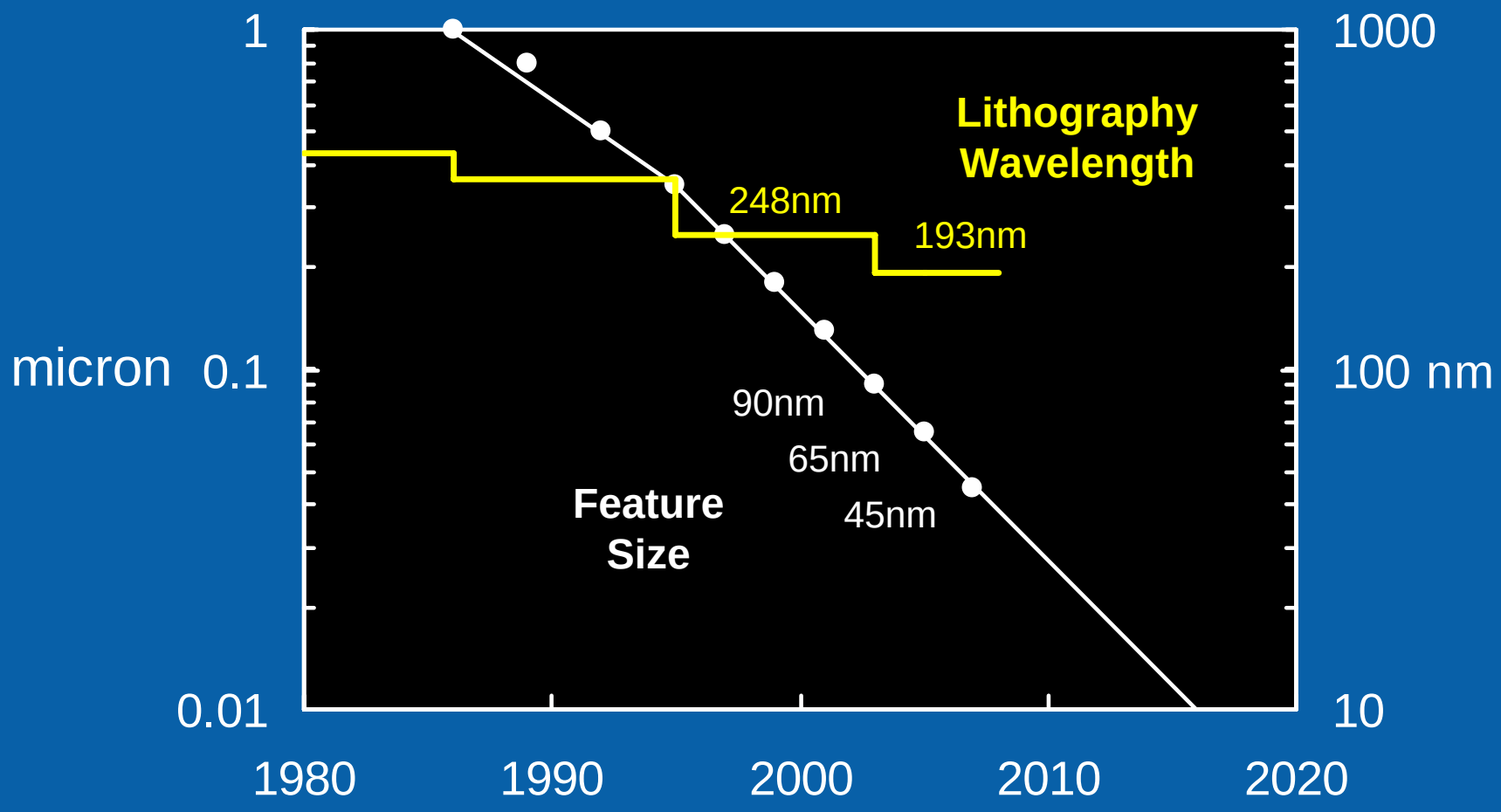
45nm Wafer



Outline

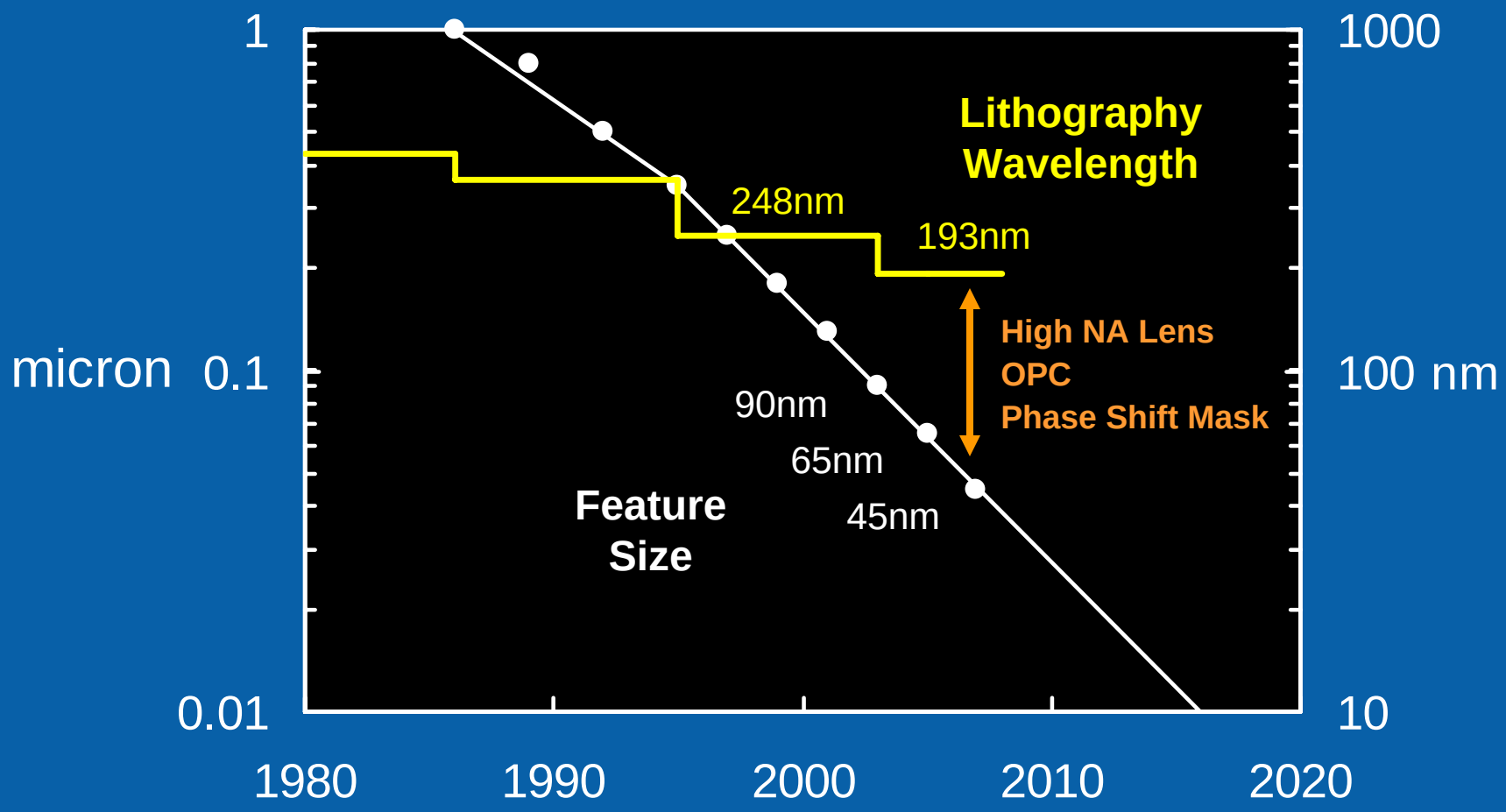
- Intel's R&D Approach
- What We've Accomplished
- Future Technology Options

Lithography



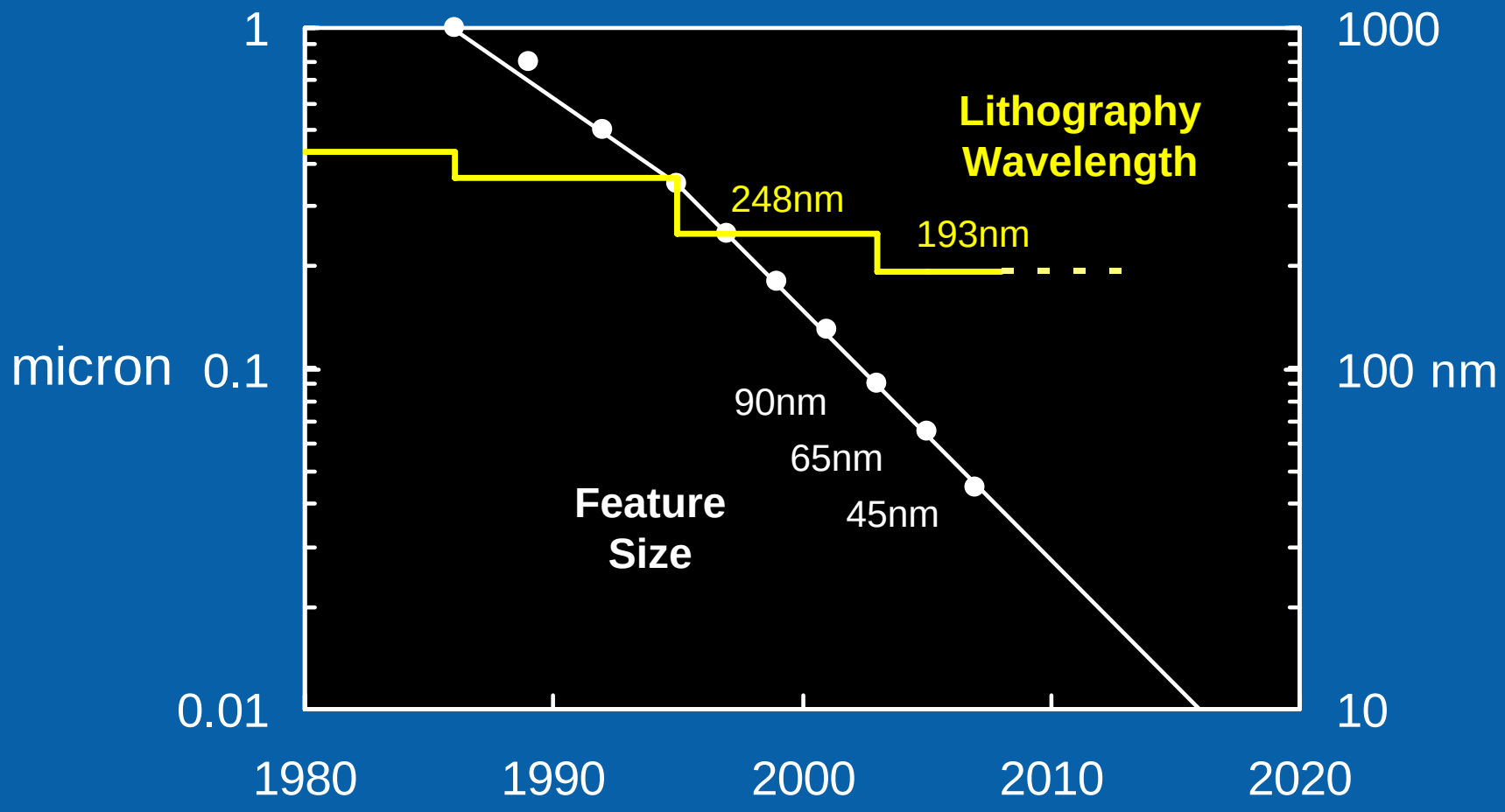
Minimum feature size is scaling faster than wavelength

Lithography



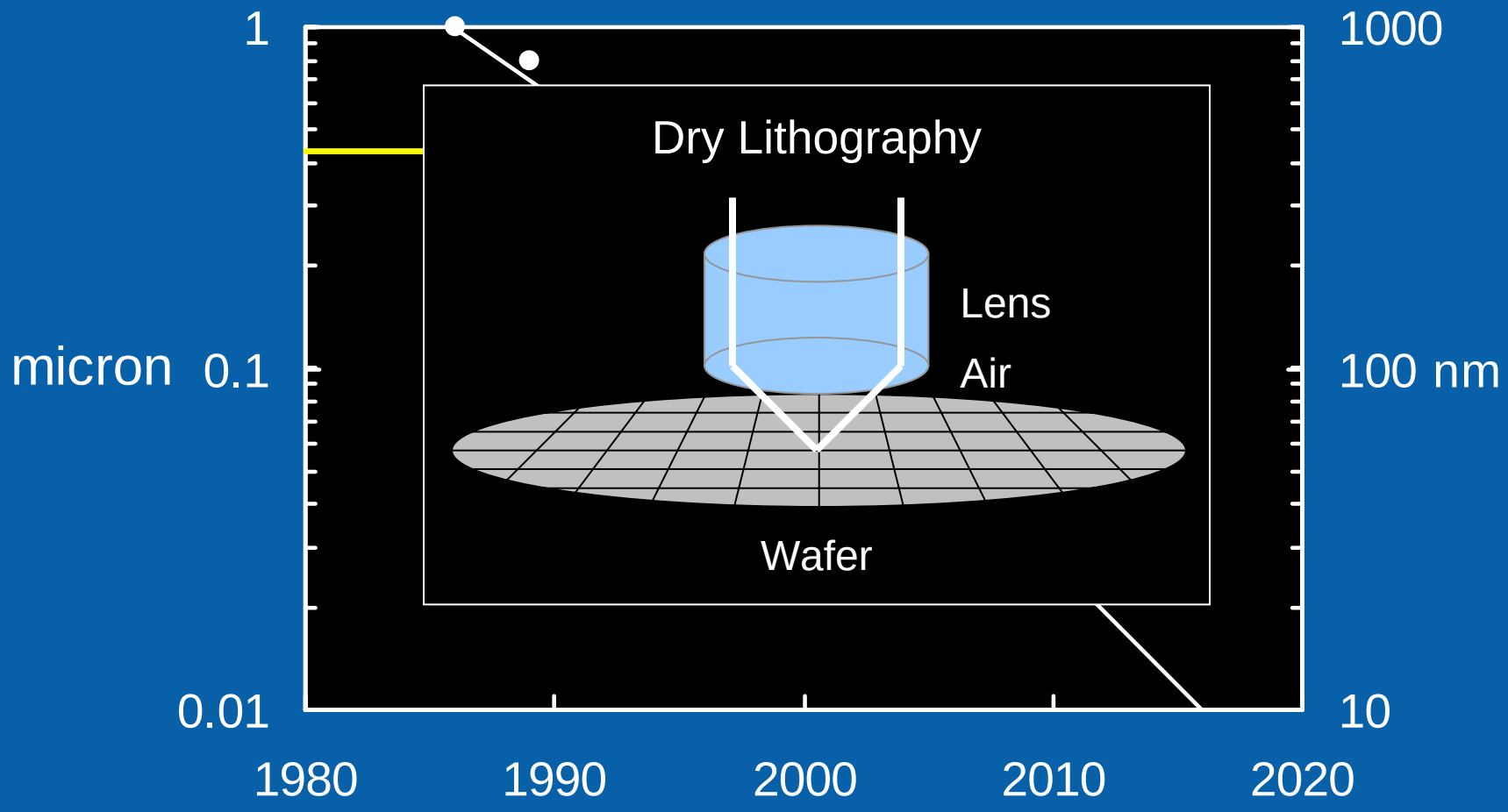
Innovations have extended 193 nm lithography to the 45 nm generation

Lithography



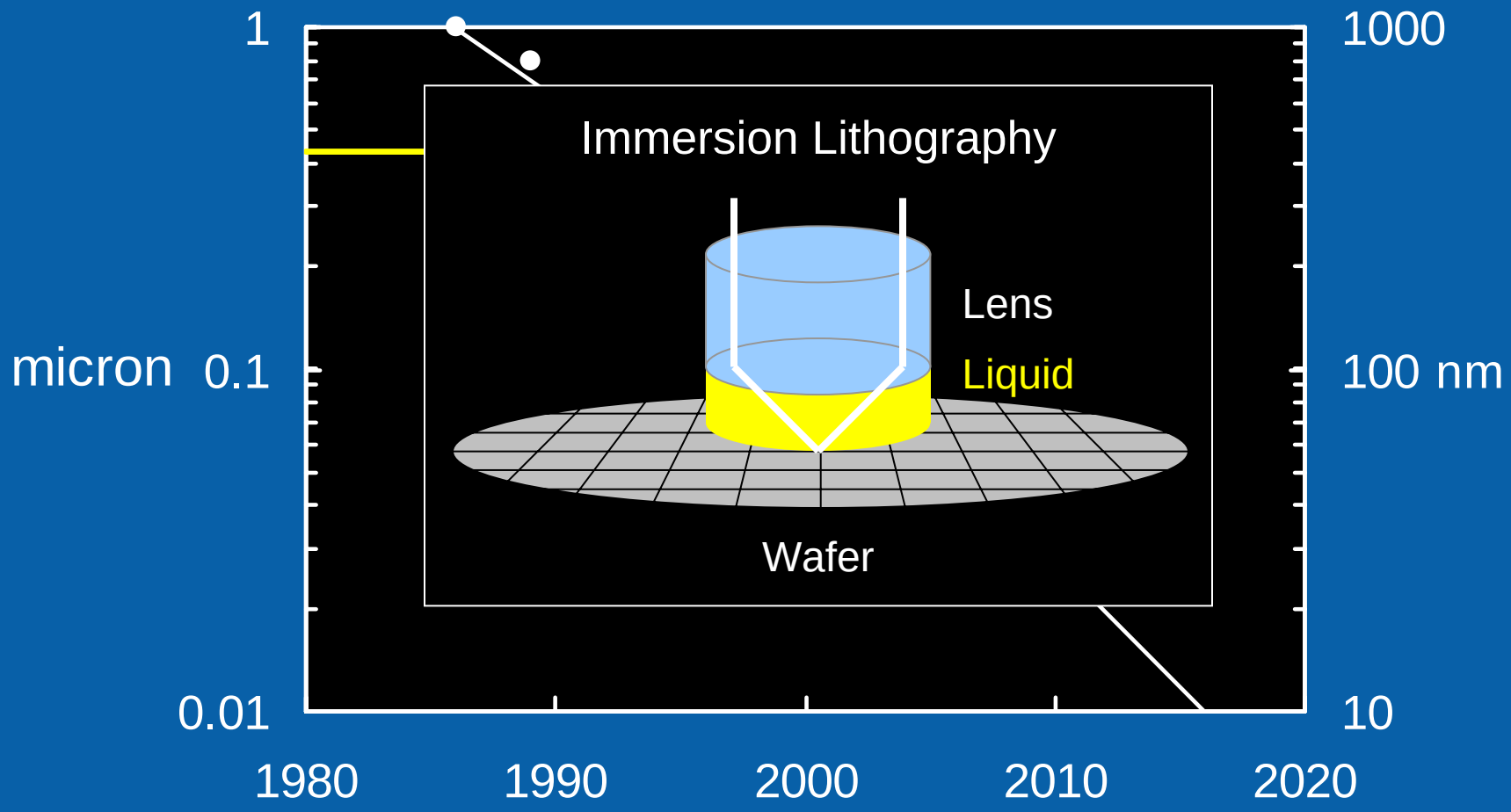
Immersion lithography is an option to extend 193 nm

Lithography



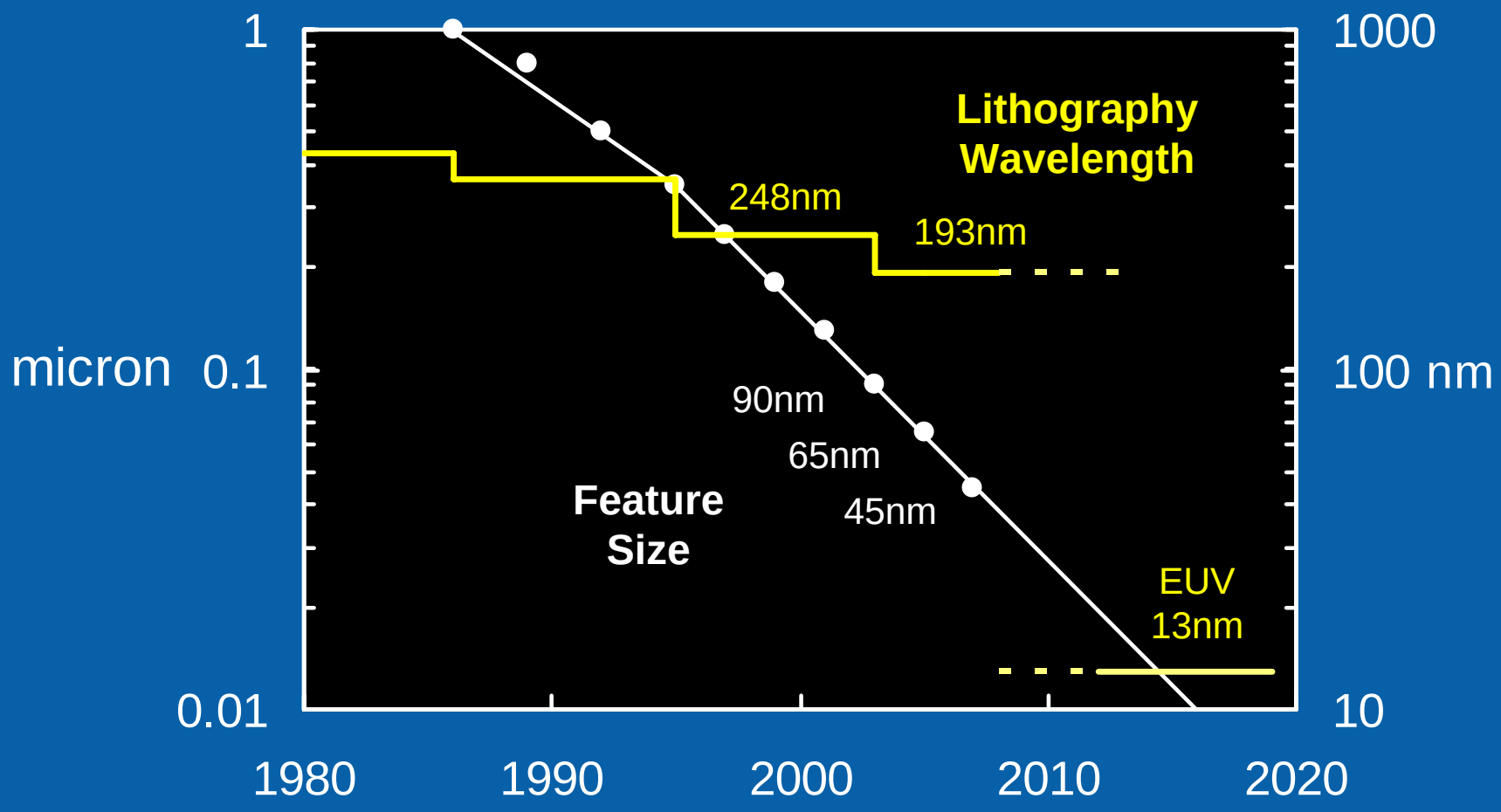
Immersion lithography is an option to extend 193 nm

Lithography



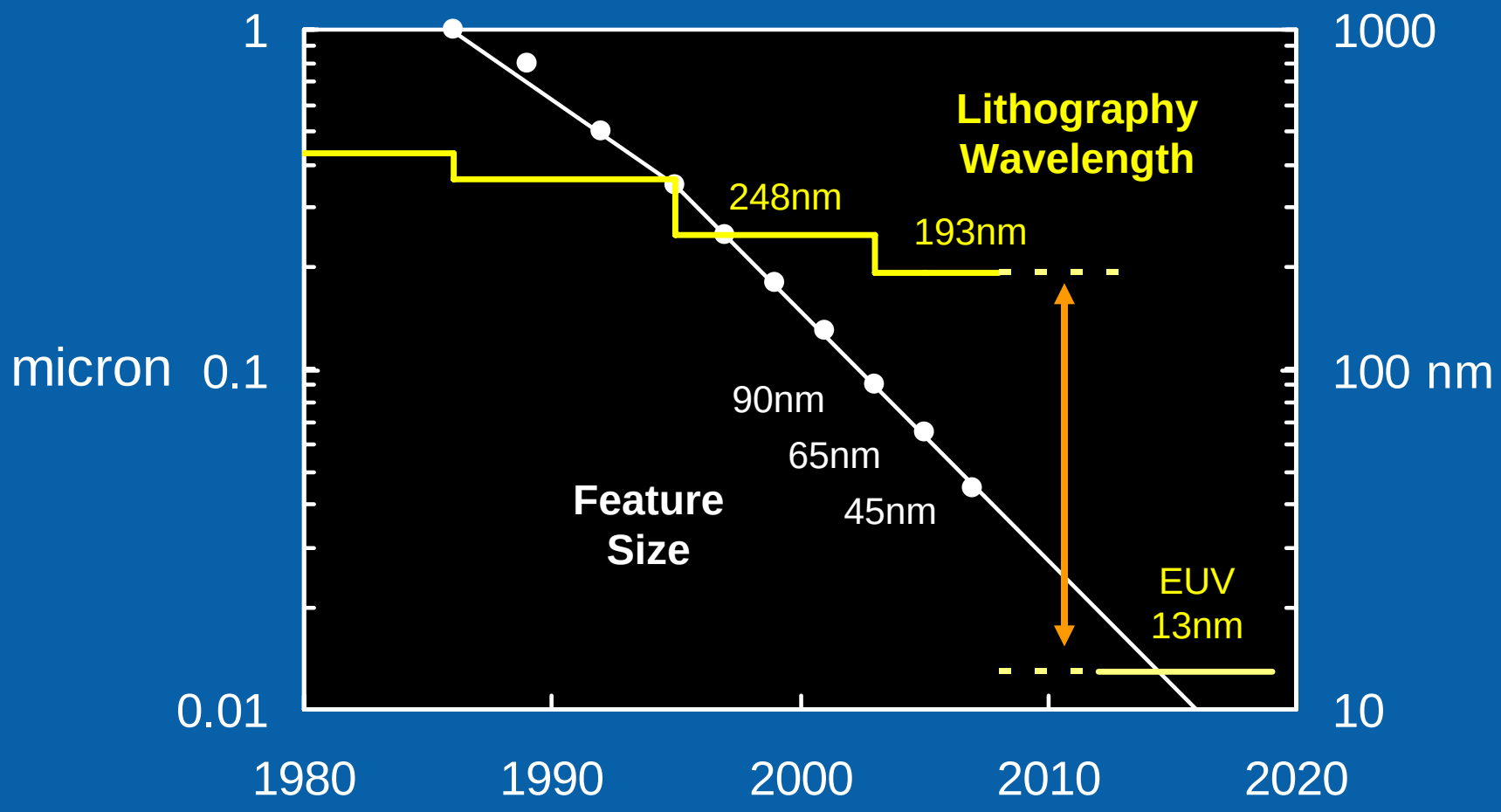
Immersion lithography is an option to extend 193 nm

Lithography



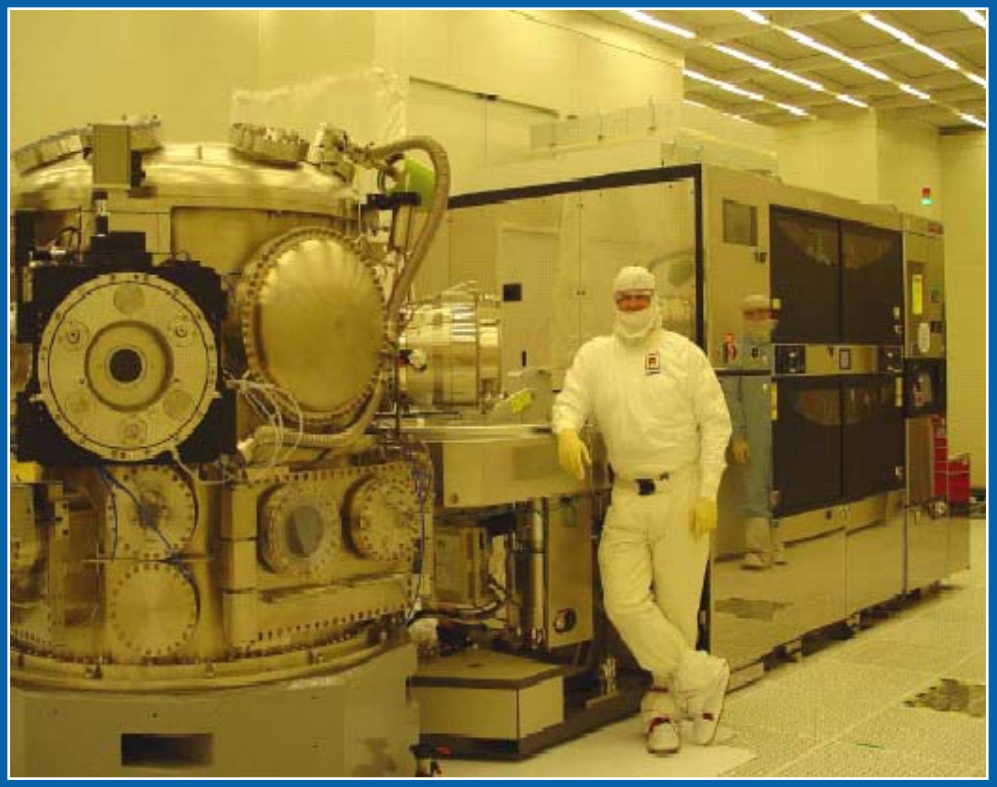
Extreme Ultraviolet is another option to extend lithography

Lithography

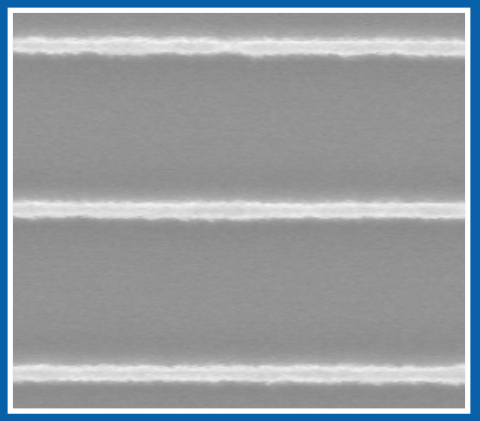


Lithography choice is based on capability, cost and readiness

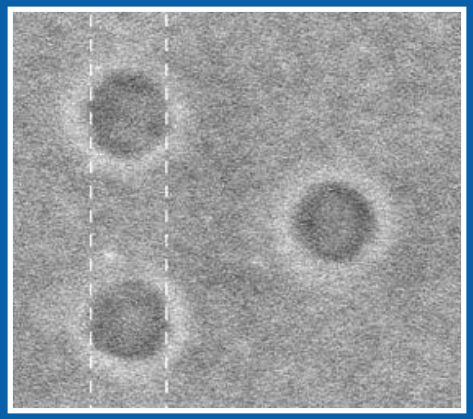
EUV Lithography



Operational EUV research tool in Oregon



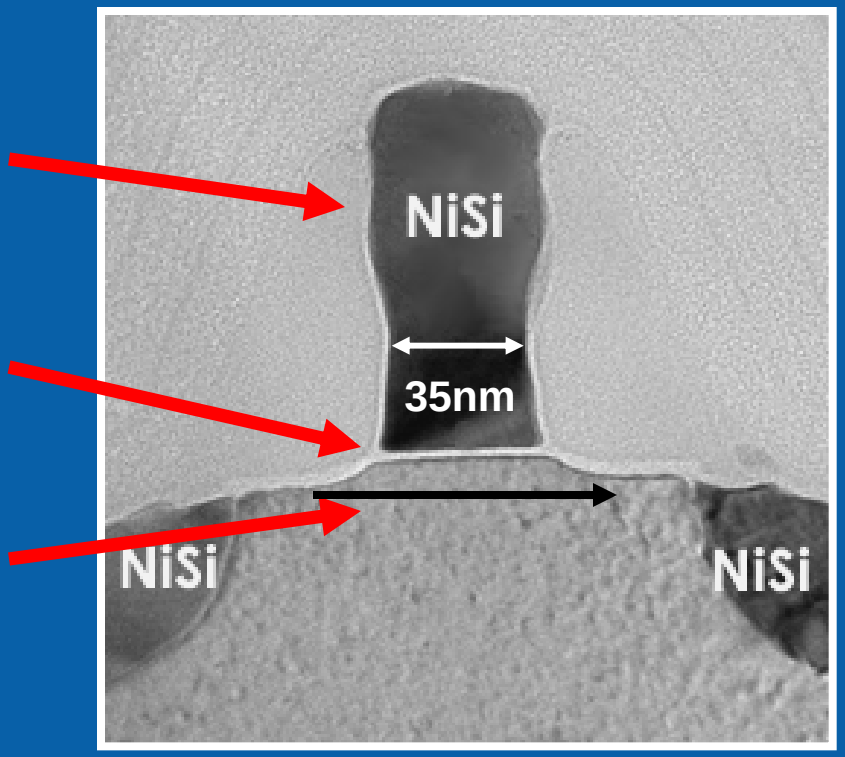
27 nm Lines



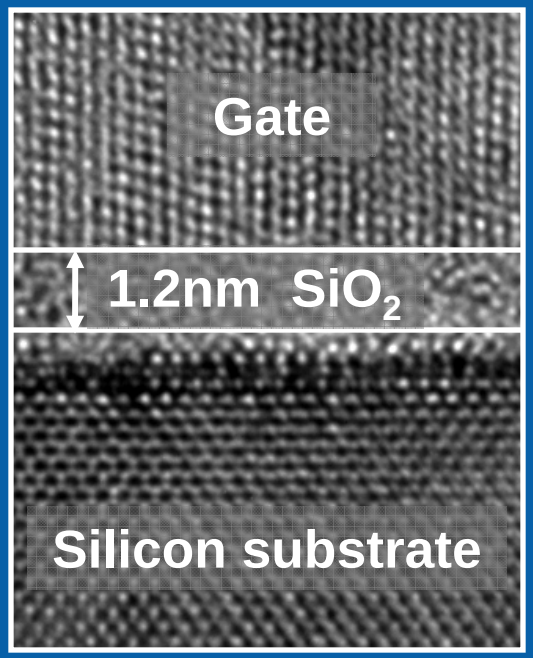
41 nm Contacts

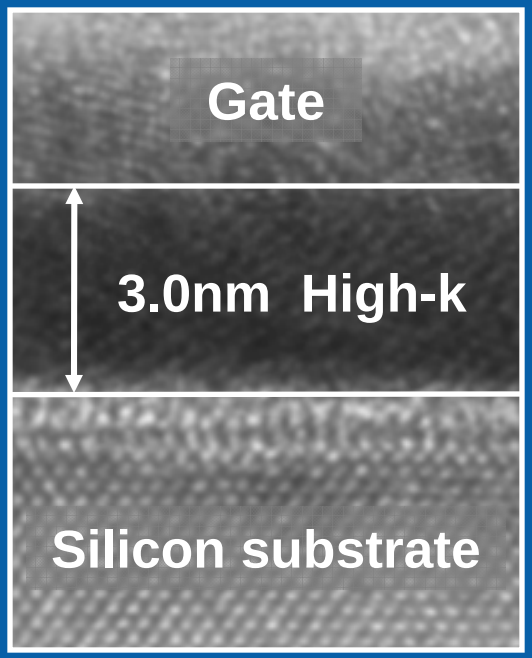
FUSI (Fully Silicided) Transistors

- Doped polysilicon gates replaced with NiSi
- NiSi (metal gate) increases gate capacitance by ~20%
- ~20% higher drive current for improved transistor performance



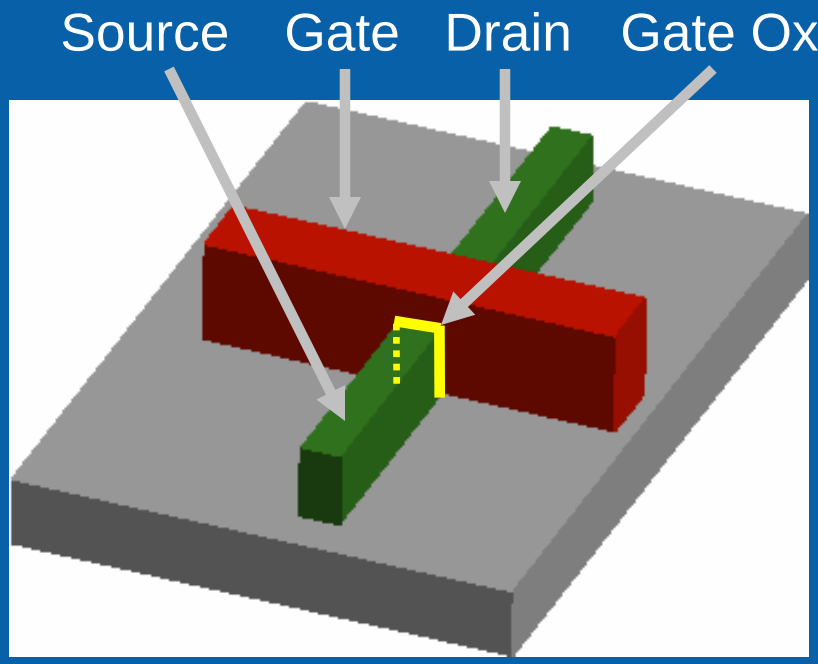
High-k Gate Dielectric

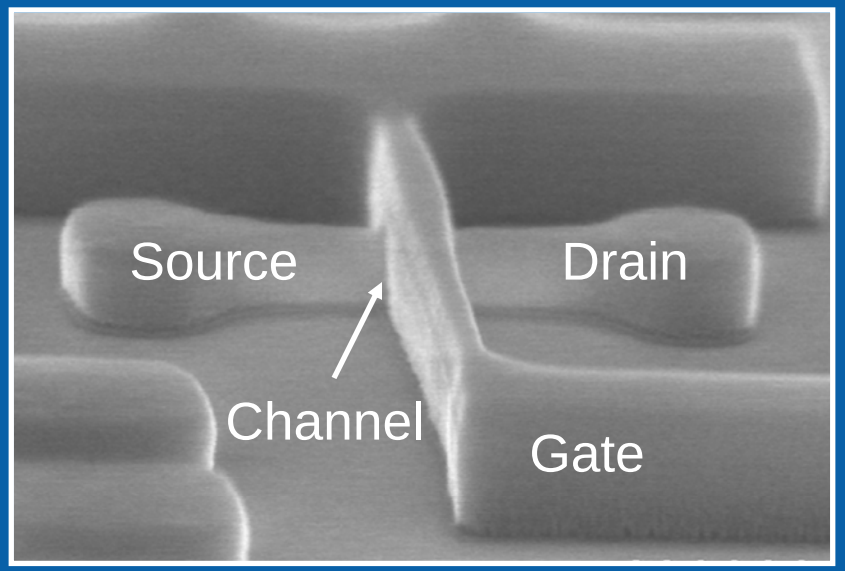




	High-k vs. SiO_2	Benefit
Capacitance	60% greater	*Faster transistors*
Gate Leakage	>100x reduction	*Cooler chips*

Tri-Gate Transistors





Transistor gate wraps around 3 sides of Si channel (Tri-Gate)

Transistor channel is “fully depleted”, different from normal bulk CMOS

Fully depleted operation reduces leakage current by up to 10x

Increasing Electron Mobility

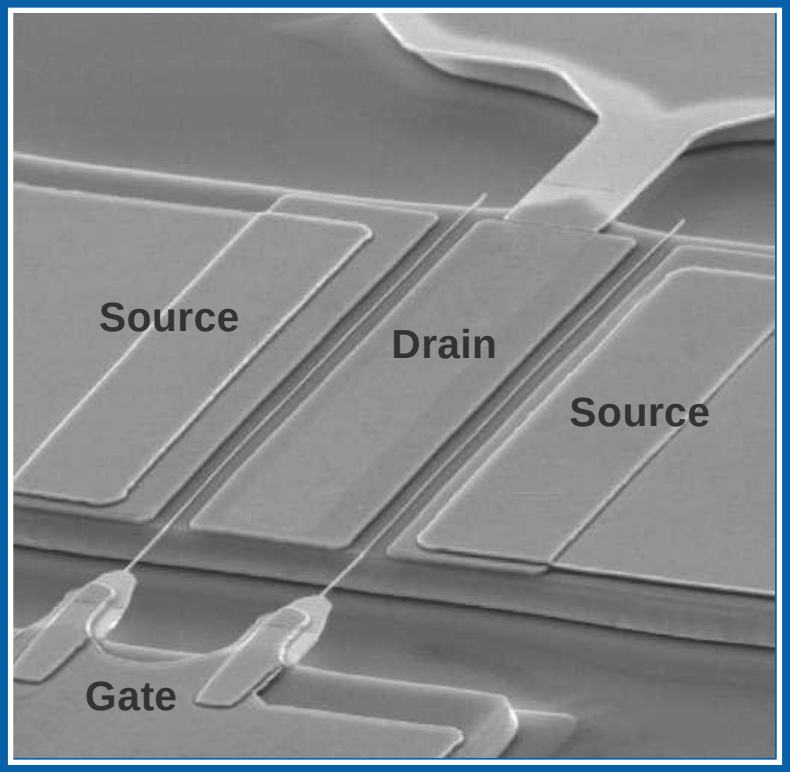
Increased electron mobility leads to higher performance and less energy consumption

	Compound Semiconductors		
Si	GaAs	InAs	InSb
1	8	33	50

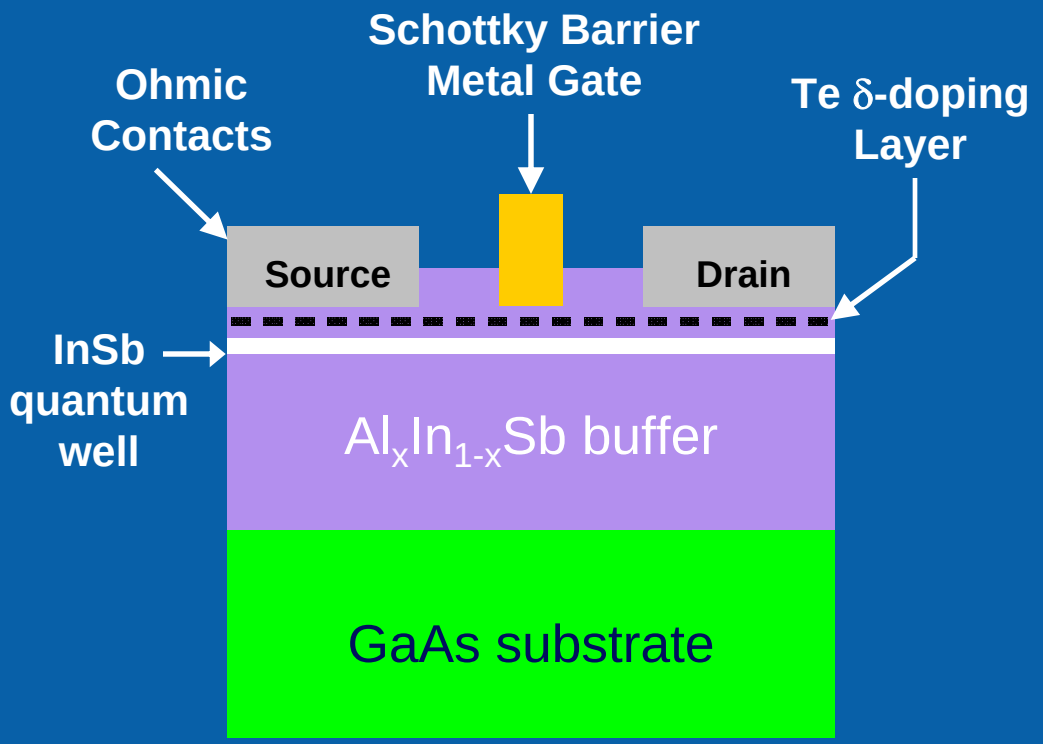
Compound semiconductors have higher electron mobility than Si

InSb (indium antimonide) is highest of all

InSb Quantum Well Transistors

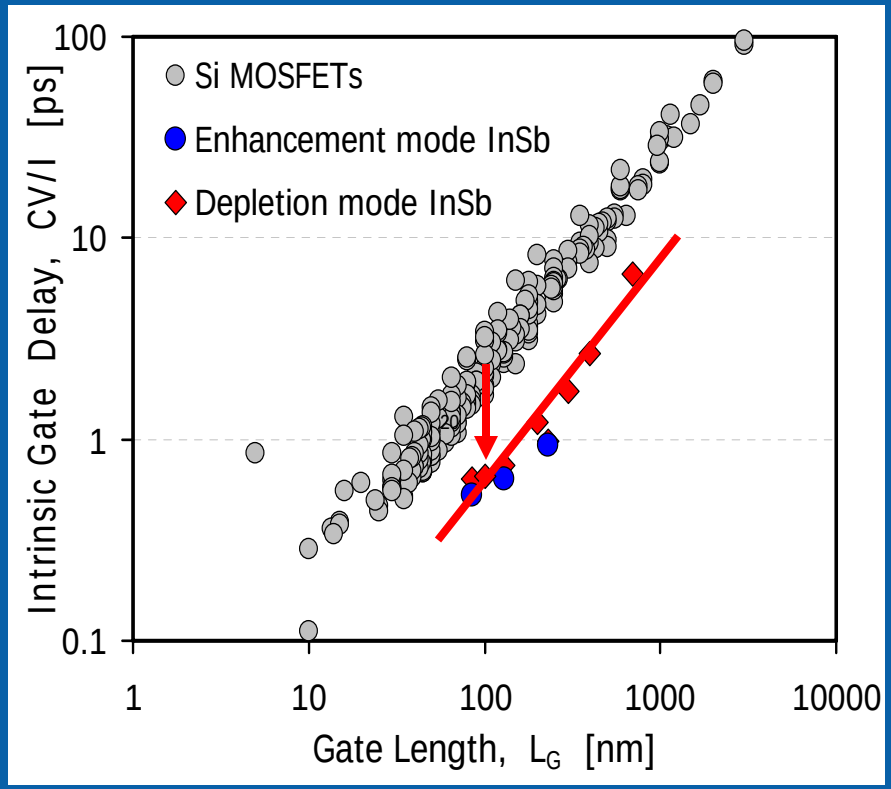


Two gate finger InSb QWFET

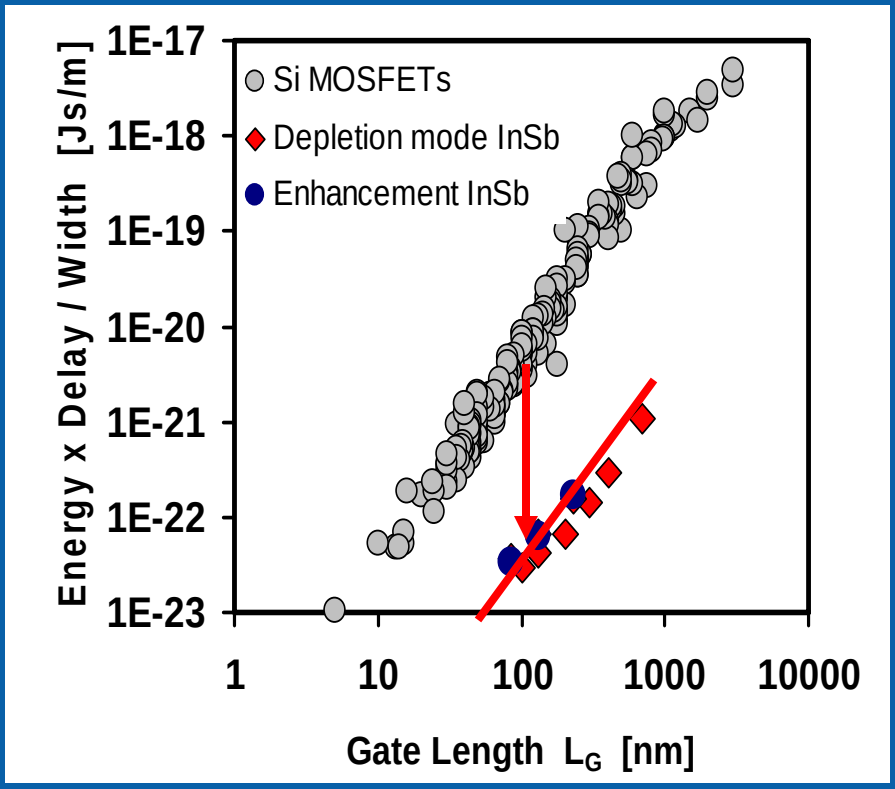


Enhancement InSb QWFET

Benchmarking InSb Transistors



InSb QWFETs have ~4x faster gate delay



InSb QWFETs have ~100x lower energy x delay

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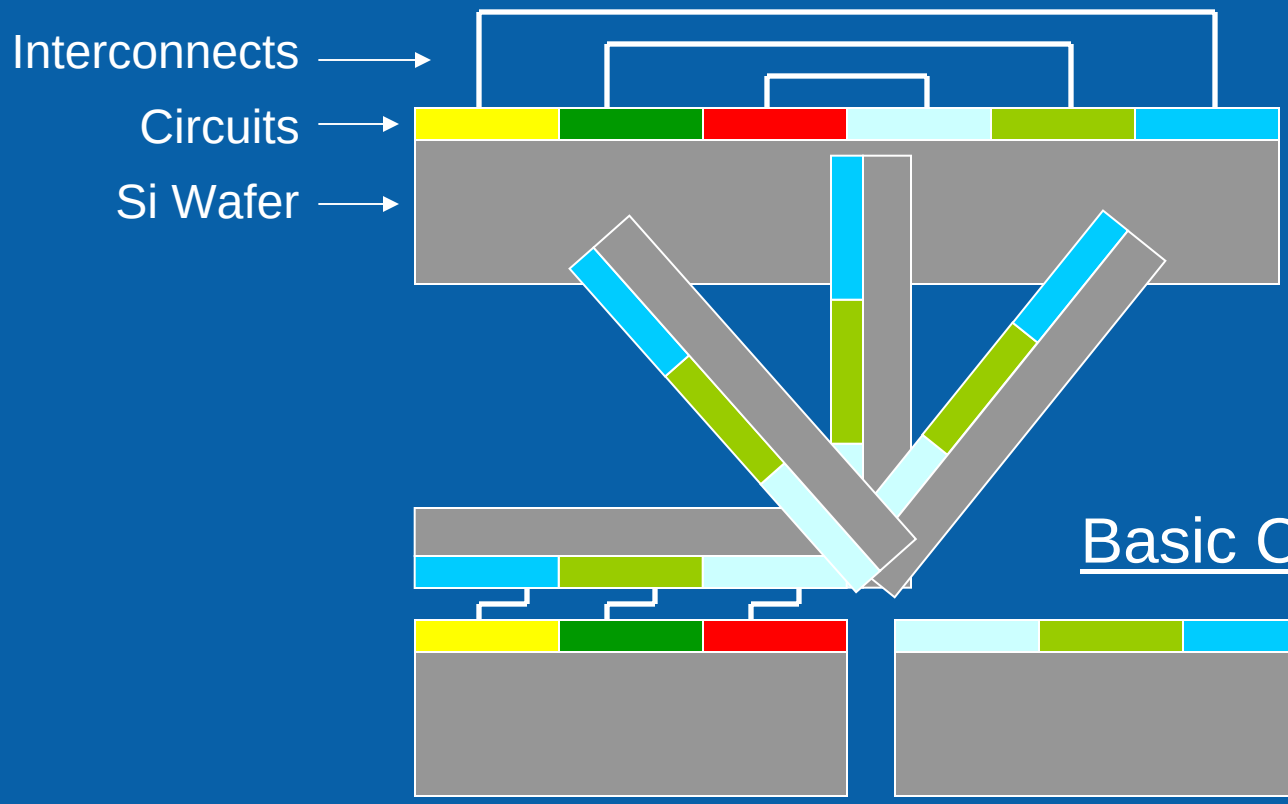
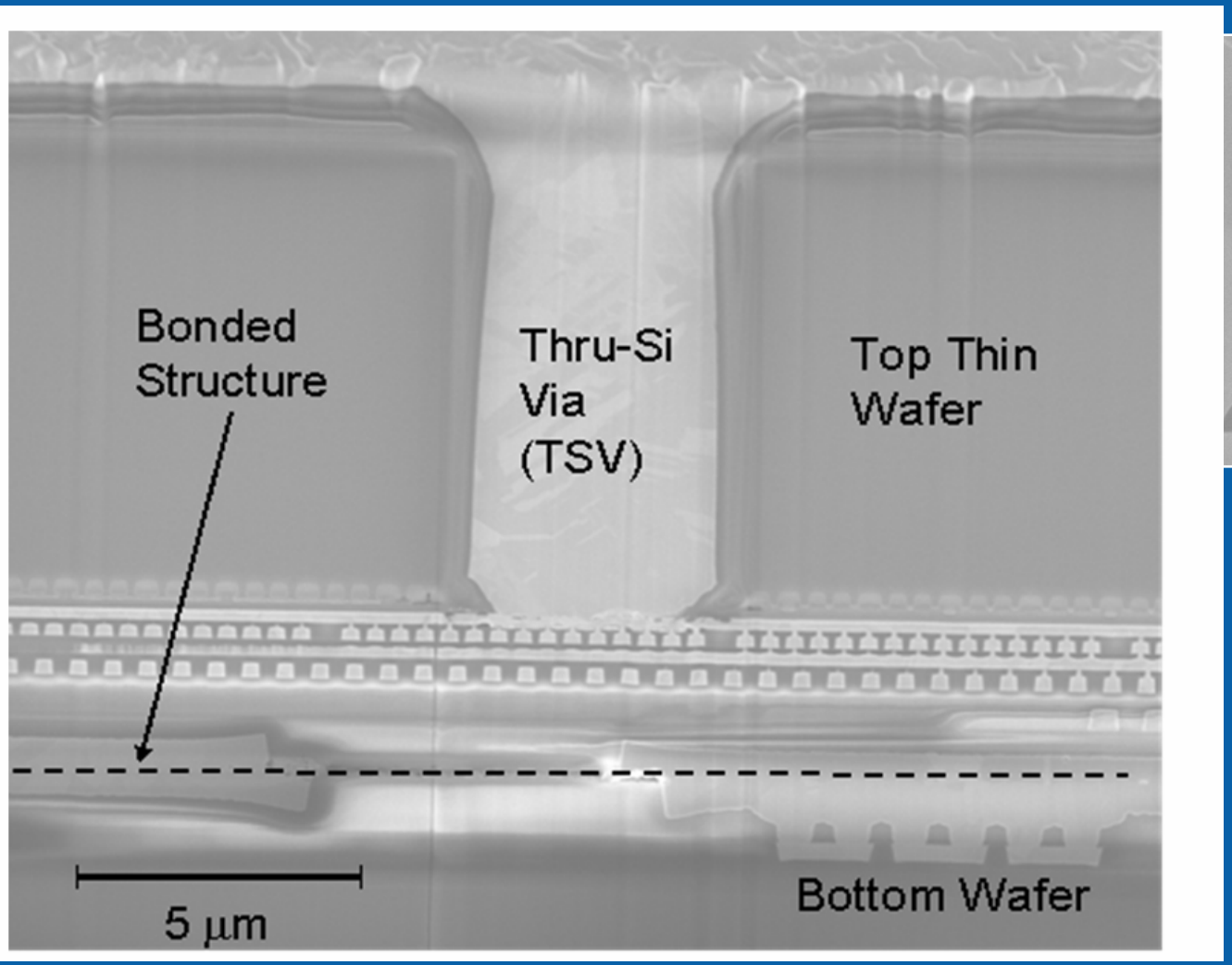
Chip Stacking Can Reduce Interconnect Lengths

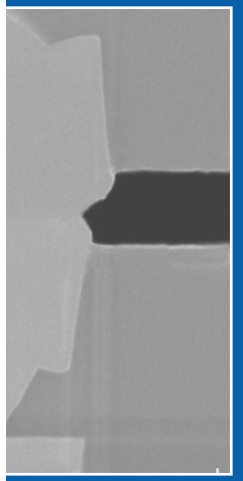


Basic Concept

t reduces
gths

3D Interconnects Research





Innovation-Enabled Technology Pipeline

90 nm
2003

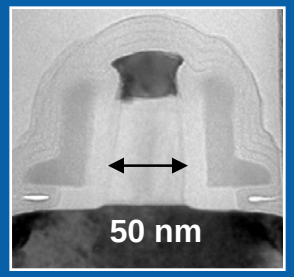
65 nm
2005

45 nm
2007

32 nm
2009

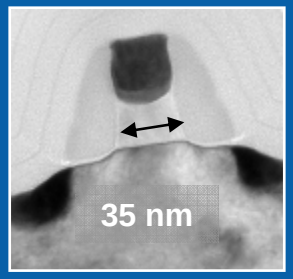
2011+

Manufacturing → Development → Research



SiGe S/D

Strained Silicon



SiGe S/D

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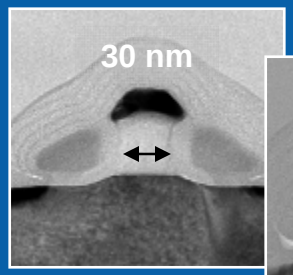

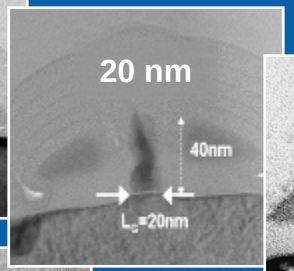

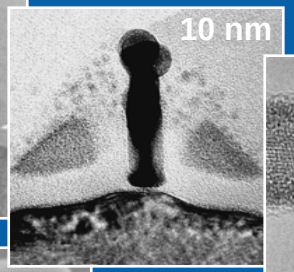

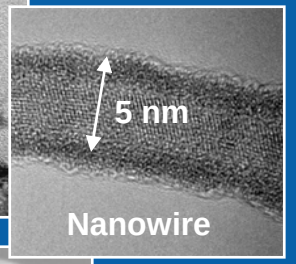

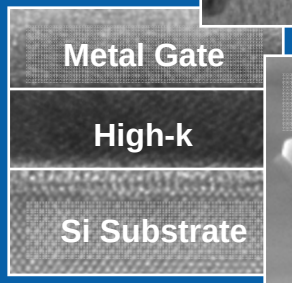

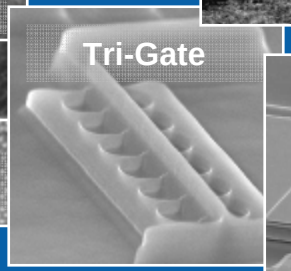

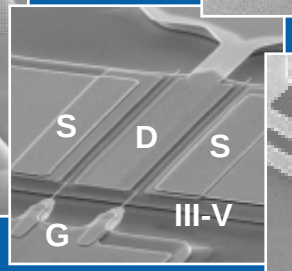

Future options subject to change

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Summary

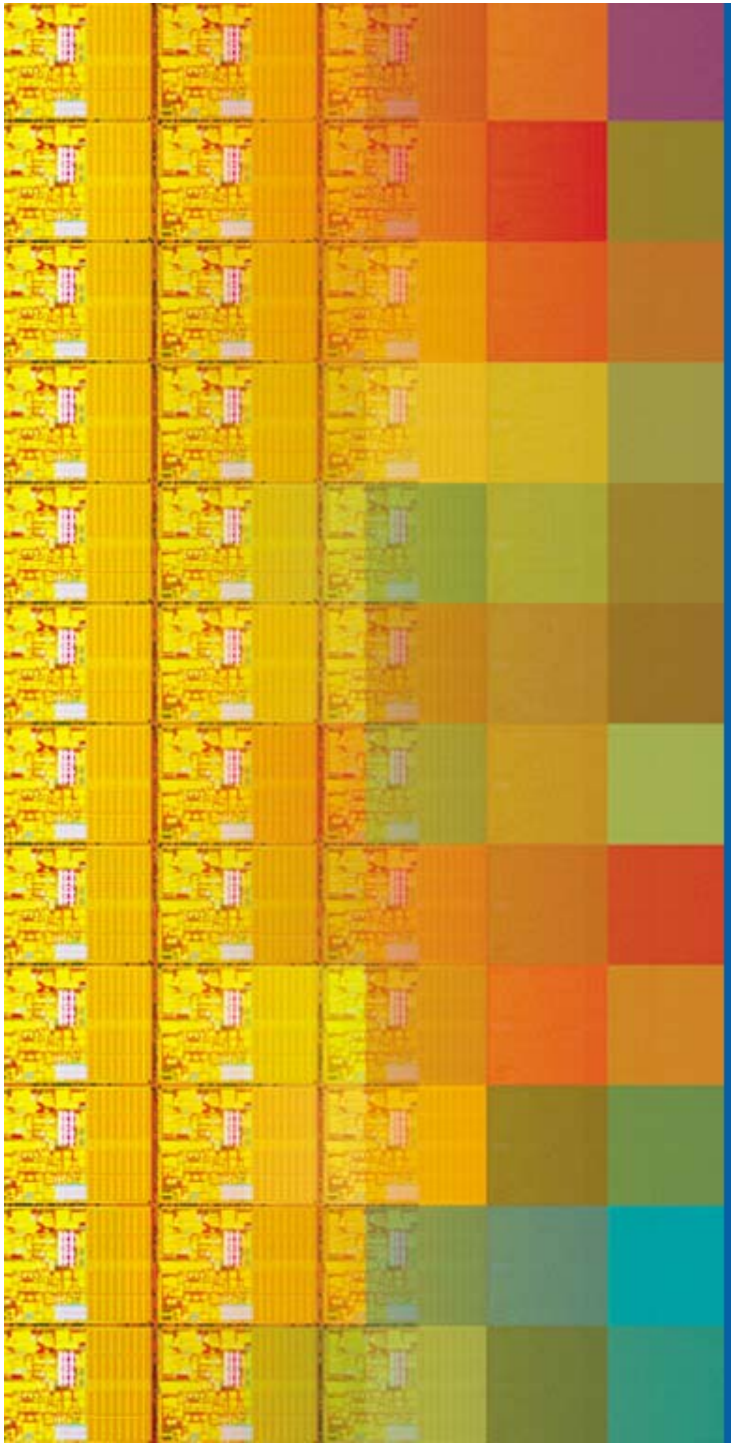
Only Intel has an effective process technology pipeline

- Follows Moore's Law on 2 year cycle
- 65nm production in Q4'05 (1 year lead)
- 45nm prototype in Q1'06
- Technology options for '07 and beyond

Process technology is an important competitive advantage for Intel platforms

- Industry-leading low leakage transistors provide a solid foundation
- Holistic approach to world class yield, energy efficient performance, and leading-edge capacity

Video



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Q&A

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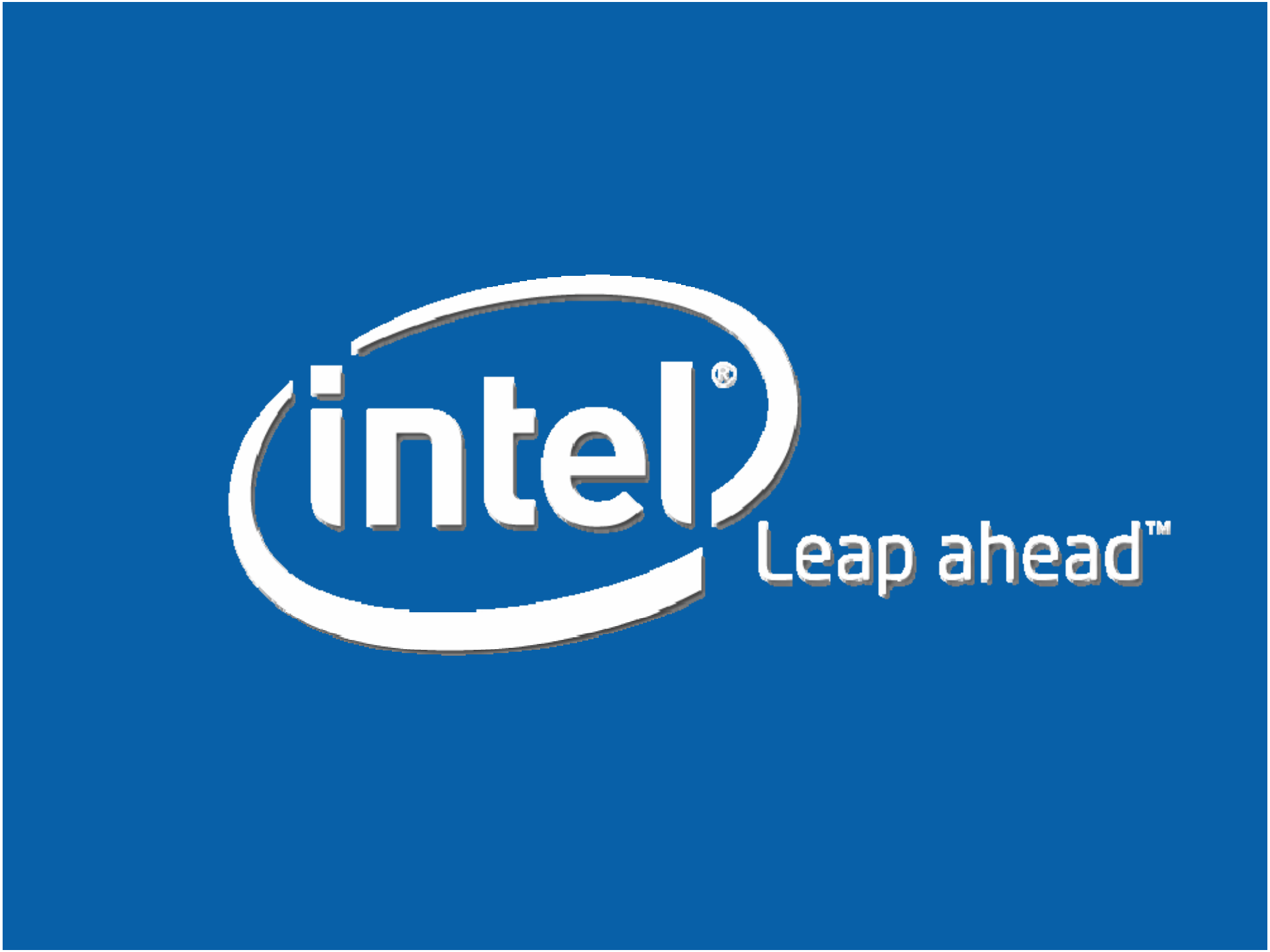
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